



# Q77H2-AD

Rev : 1.0.

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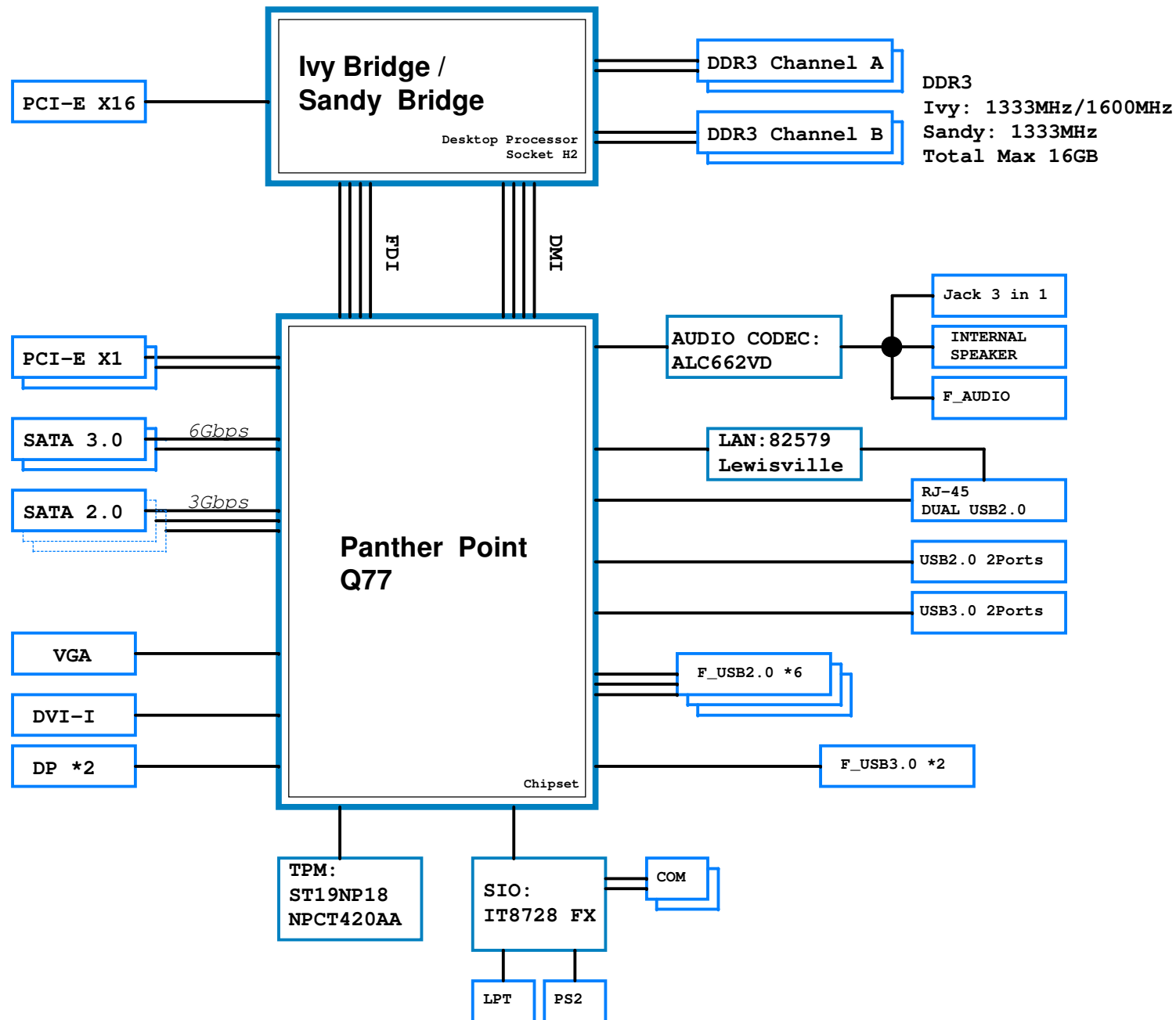
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## REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version
V.B	2011/12/13	
V1.0	2012/01/17	
V1.0.	2012/04/10	

 <b>Elitegroup Computer Systems</b>		
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## GPIO Table

### PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO27	I/O	SB_3VSB	Input	LANWAKEB for Bcm
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4S5

### IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

## Straping Table

### PCH Straping (Page.14)

#### TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

#### No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

#### On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

#### On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

#### Integrated 1.05V SUS VRM:

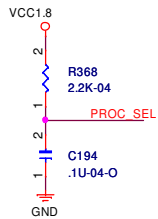
INTVRMEN	
H	Enable
L	Disable

## SIO IT8728F D/EX Straping (Page.28)

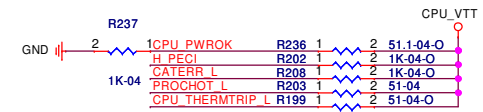
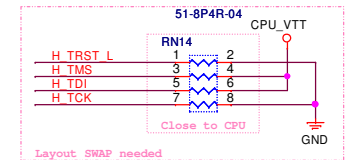
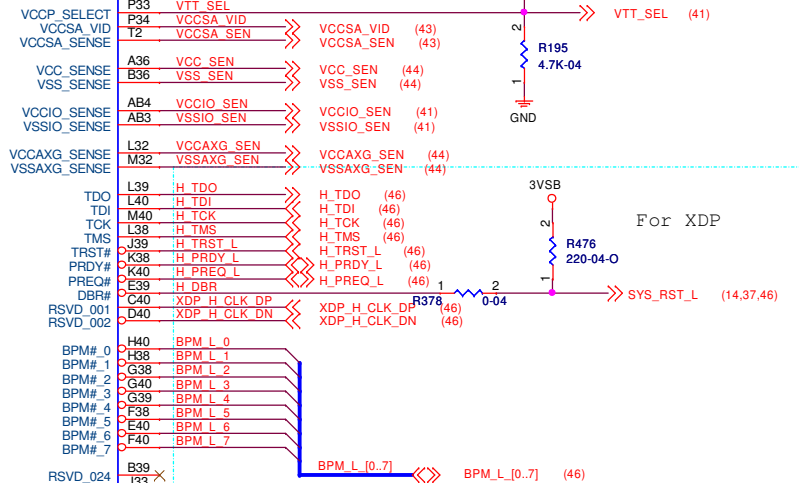
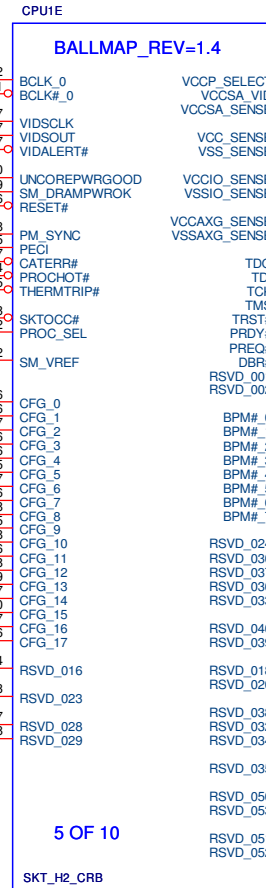
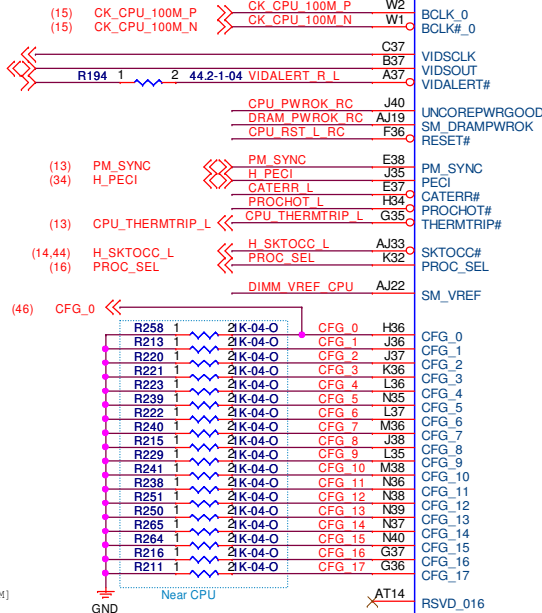
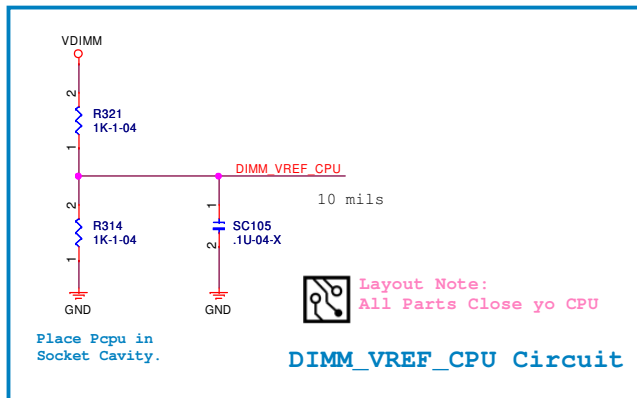
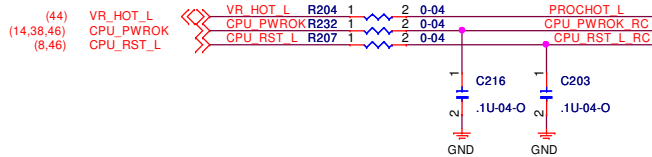
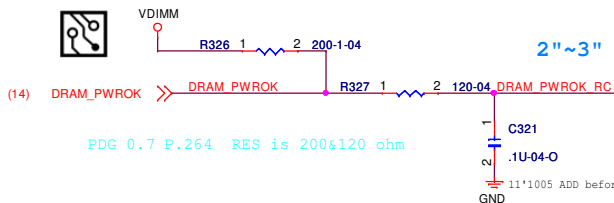
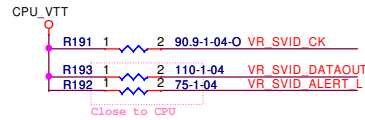
### Power-On Strapping

	Symbol	Value	Description
JP1 Pin-48	DSW_EUP_SEL	1	EUP
		0	DSW
JP2 Pin-122	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK
JP3 Pin-124	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
		0	EC Index 63h/6Bh/73h is 00h
JP4 Pin-126	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence
JP5 Pin-29	UOVMODE_SEL	1	Notice Mode (Default)
	OV/UV	0	Force Mode





DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1 X16	1	1
2 X8	0	1

CFG[5:6]:  
11=DEFAULT X16,  
01=2X8,  
10=RESERVED,  
00=X8,X4,X4

**ECS Elitegroup Computer Systems**

Title: **CPU - MISC**

Size: Custom Document Number: **Q77H2-AD** Rev: 1.0

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CFG\_0..17 HAVE INTERNAL PULL-UPS

(9)	M_DATA_A[0..63]	←	M_DATA A[0..63]
(9)	M_DQS_A_P[0..7]	←	M DQS A P[0..7]
(9)	M_DQS_A_N[0..7]	←	M DQS A N[0..7]
(9)	M_MA_A[0..15]	←	M MA A[0..15]
(9)	M_MA_A[0..15]	←	M BS A[0..2]
(9)	M_BS_A[0..2]	←	M CS A L[0..3]
(9)	M_CS_A_L[0..3]	←	M_CKE A[0..3]
(9)	M_CKE_A[0..3]	←	M_ODT A[0..3]
(9)	M_ODT_A[0..3]	←	M_CLK A P[0..3]
(9)	M_CLK_A_P[0..3]	←	M_CLK A N[0..3]
(9)	M_CLK_A_N[0..3]	←	M WE A L
(9)	M_WE_A_L	←	M CAS A L
(9)	M_CAS_A_L	←	M RAS A L
(9)	M_RAS_A_L	←	

DDR3 CH.A

(9,10) DDR3\_DRAMRST\_L ← DDR3\_DRAMRST\_L

(10)	M_DATA_B[0..63]	←	M_DATA B[0..63]
(10)	M_DQS_B_P[0..7]	←	M DQS B P[0..7]
(10)	M_DQS_B_N[0..7]	←	M DQS B N[0..7]
(10)	M_MA_B[0..15]	←	M MA B[0..15]
(10)	M_MA_B[0..15]	←	M BS B[0..2]
(10)	M_BS_B[0..2]	←	M CS B L[0..3]
(10)	M_CS_B_L[0..3]	←	M_CKE B[0..3]
(10)	M_CKE_B[0..3]	←	M_ODT B[0..3]
(10)	M_ODT_B[0..3]	←	M_CLK B P[0..3]
(10)	M_CLK_B_P[0..3]	←	M_CLK B N[0..3]
(10)	M_CLK_B_N[0..3]	←	M WE B L
(10)	M_WE_B_L	←	M CAS B L
(10)	M_CAS_B_L	←	M RAS B L
(10)	M_RAS_B_L	←	

DDR3 CH.B

CPU1C			
BALLMAP_REV=1.4			
M_DATA A0	AJ3	SA_DQ_0	AV27
M_DATA A1	AJ4	SA_DQ_1	AV24
M_DATA A2	AL3	SA_DQ_2	AW24
M_DATA A3	AL4	SA_DQ_3	AW23
M_DATA A4	AJ2	SA_DQ_4	AV23
M_DATA A5	AJ1	SA_DQ_5	AT24
M_DATA A6	AL1	SA_DQ_6	AV23
M_DATA A7	AL1	SA_DQ_7	AV22
M_DATA A8	AN1	SA_DQ_8	AT22
M_DATA A9	AN4	SA_DQ_9	AV28
M_DATA A10	AR3	SA_DQ_10	AT21
M_DATA A11	AR4	SA_DQ_11	AW32
M_DATA A12	AN2	SA_DQ_12	AU22
M_DATA A13	AN3	SA_DQ_13	AV22
M_DATA A14	AR2	SA_DQ_14	AT22
M_DATA A15	AR1	SA_DQ_15	AV28
M_DATA A16	AV2	SA_DQ_16	AT21
M_DATA A17	AV3	SA_DQ_17	AW32
M_DATA A18	AV5	SA_DQ_18	AU22
M_DATA A19	AW5	SA_DQ_19	AV22
M_DATA A20	AU2	SA_DQ_20	AT22
M_DATA A21	AU3	SA_DQ_21	AW32
M_DATA A22	AU5	SA_DQ_22	AU22
M_DATA A23	AY7	SA_DQ_23	AV22
M_DATA A24	AY7	SA_DQ_24	AT22
M_DATA A25	AU7	SA_DQ_25	AW32
M_DATA A26	AV9	SA_DQ_26	AU22
M_DATA A27	AU9	SA_DQ_27	AV22
M_DATA A28	AV7	SA_DQ_28	AT22
M_DATA A29	AW7	SA_DQ_29	AW32
M_DATA A30	AW9	SA_DQ_30	AU22
M_DATA A31	AY9	SA_DQ_31	AV22
M_DATA A32	AU35	SA_DQ_32	AT22
M_DATA A33	AW37	SA_DQ_33	AW32
M_DATA A34	AU39	SA_DQ_34	AU22
M_DATA A35	AU36	SA_DQ_35	AV22
M_DATA A36	AW35	SA_DQ_36	AT22
M_DATA A37	AY36	SA_DQ_37	AW32
M_DATA A38	AU38	SA_DQ_38	AU22
M_DATA A39	AU37	SA_DQ_39	AV22
M_DATA A40	AR40	SA_DQ_40	AT22
M_DATA A41	AR37	SA_DQ_41	AW32
M_DATA A42	AN38	SA_DQ_42	AU22
M_DATA A43	AN37	SA_DQ_43	AV22
M_DATA A44	AR39	SA_DQ_44	AT22
M_DATA A45	AR38	SA_DQ_45	AW32
M_DATA A46	AR39	SA_DQ_46	AU22
M_DATA A47	AN40	SA_DQ_47	AV22
M_DATA A48	AL40	SA_DQ_48	AT22
M_DATA A49	AL37	SA_DQ_49	AW32
M_DATA A50	AJ38	SA_DQ_50	AU22
M_DATA A51	AJ37	SA_DQ_51	AV22
M_DATA A52	AL39	SA_DQ_52	AT22
M_DATA A53	AL38	SA_DQ_53	AW32
M_DATA A54	AJ39	SA_DQ_54	AU22
M_DATA A55	AJ40	SA_DQ_55	AV22
M_DATA A56	AG40	SA_DQ_56	AT22
M_DATA A57	AG37	SA_DQ_57	AW32
M_DATA A58	AE38	SA_DQ_58	AU22
M_DATA A59	AE37	SA_DQ_59	AV22
M_DATA A60	AG39	SA_DQ_60	AT22
M_DATA A61	AG38	SA_DQ_61	AW32
M_DATA A62	AE39	SA_DQ_62	AU22
M_DATA A63	AE40	SA_DQ_63	AV22
M_DQS A P0	AK3	SA_DQS_0	AV13
M_DQS A P1	AP3	SA_DQS_1	AV12
M_DQS A P2	AV4	SA_DQS_2	AU12
M_DQS A P3	AV8	SA_DQS_3	AU14
M_DQS A P4	AV37	SA_DQS_4	AW13
M_DQS A P5	AP38	SA_DQS_5	AV13
M_DQS A P6	AK38	SA_DQS_6	AU11
M_DQS A P7	AF38	SA_DQS_7	AV12
M_DQS A N0	AK2	SA_DQS#_0	AW12
M_DQS A N1	AP2	SA_DQS#_1	
M_DQS A N2	AV4	SA_DQS#_2	
M_DQS A N3	AV8	SA_DQS#_3	
M_DQS A N4	AV37	SA_DQS#_4	
M_DQS A N5	AP38	SA_DQS#_5	
M_DQS A N6	AK38	SA_DQS#_6	
M_DQS A N7	AF38	SA_DQS#_7	

SM\_DRAMRST#

SA\_DQS\_8

SA\_ECC\_CB\_0  
SA\_ECC\_CB\_1  
SA\_ECC\_CB\_2  
SA\_ECC\_CB\_3  
SA\_ECC\_CB\_4  
SA\_ECC\_CB\_5  
SA\_ECC\_CB\_6  
SA\_ECC\_CB\_7

DDR\_0  
3 OF 10

SKT\_H2\_CRB

DDR3 CH.A

CPU1D			
BALLMAP_REV=1.4			
M_DATA B0	AG7	SB_DQ_0	AK24
M_DATA B1	AG8	SB_DQ_1	AM20
M_DATA B2	AJ9	SB_DQ_2	AM19
M_DATA B3	AJ8	SB_DQ_3	AK18
M_DATA B4	AG5	SB_DQ_4	AP19
M_DATA B5	AG6	SB_DQ_5	AP18
M_DATA B6	AL6	SB_DQ_6	AM18
M_DATA B7	AJ7	SB_DQ_7	AL18
M_DATA B8	AL7	SB_DQ_8	AN18
M_DATA B9	AM7	SB_DQ_9	AY17
M_DATA B10	AM10	SB_DQ_10	AN23
M_DATA B11	AL10	SB_DQ_11	AU17
M_DATA B12	AL6	SB_DQ_12	AT18
M_DATA B13	AL9	SB_DQ_13	AR26
M_DATA B14	AM9	SB_DQ_14	AY16
M_DATA B15	AP7	SB_DQ_15	AV16
M_DATA B16	AP7	SB_DQ_16	
M_DATA B17	AP10	SB_DQ_17	AR25
M_DATA B18	AR10	SB_DQ_18	AK25
M_DATA B19	AP6	SB_DQ_19	AP24
M_DATA B20	AP6	SB_DQ_20	
M_DATA B21	AP6	SB_DQ_21	
M_DATA B22	AP9	SB_DQ_22	AP23
M_DATA B23	AP9	SB_DQ_23	AM24
M_DATA B24	AM12	SB_DQ_24	AW17
M_DATA B25	AM13	SB_DQ_25	
M_DATA B26	AR13	SB_DQ_26	
M_DATA B27	AP13	SB_DQ_27	AN25
M_DATA B28	AL12	SB_DQ_28	AN26
M_DATA B29	AL12	SB_DQ_29	AL25
M_DATA B30	AR12	SB_DQ_30	AT26
M_DATA B31	AP12	SB_DQ_31	
M_DATA B32	AR28	SB_DQ_32	
M_DATA B33	AR29	SB_DQ_33	
M_DATA B34	AL28	SB_DQ_34	AU16
M_DATA B35	AL29	SB_DQ_35	AY15
M_DATA B36	AP28	SB_DQ_36	AW15
M_DATA B37	AP29	SB_DQ_37	AV15
M_DATA B38	AM28	SB_DQ_38	
M_DATA B39	AM29	SB_DQ_39	
M_DATA B40	AP32	SB_DQ_40	
M_DATA B41	AP31	SB_DQ_41	
M_DATA B42	AP35	SB_DQ_42	AL26
M_DATA B43	AP34	SB_DQ_43	AP26
M_DATA B44	AR32	SB_DQ_44	AM26
M_DATA B45	AR31	SB_DQ_45	AK26
M_DATA B46	AR35	SB_DQ_46	
M_DATA B47	AR34	SB_DQ_47	
M_DATA B48	AM32	SB_DQ_48	
M_DATA B49	AM31	SB_DQ_49	
M_DATA B50	AL35	SB_DQ_50	AL21
M_DATA B51	AL32	SB_DQ_51	AL22
M_DATA B52	AM34	SB_DQ_52	AL20
M_DATA B53	AL31	SB_DQ_53	AK20
M_DATA B54	AM35	SB_DQ_54	AL23
M_DATA B55	AL34	SB_DQ_55	AM22
M_DATA B56	AH35	SB_DQ_56	AP21
M_DATA B57	AH34	SB_DQ_57	AN21
M_DATA B58	AE34	SB_DQ_58	
M_DATA B59	AE35	SB_DQ_59	
M_DATA B60	AJ35	SB_DQ_60	
M_DATA B61	AJ34	SB_DQ_61	
M_DATA B62	AF33	SB_DQ_62	
M_DATA B63	AF35	SB_DQ_63	
M_DQS B P0	AH7	SB_DQS_0	AN16
M_DQS B P1	AM8	SB_DQS_1	AN15
M_DQS B P2	AR8	SB_DQS_2	
M_DQS B P3	AN13	SB_DQS_3	
M_DQS B P4	AN29	SB_DQS_4	AL16
M_DQS B P5	AP33	SB_DQS_5	AM16
M_DQS B P6	AL33	SB_DQS_6	AP16
M_DQS B P7	AG35	SB_DQS_7	AR16
M_DQS B N0	AH6	SB_DQS#_0	AL15
M_DQS B N1	AL8	SB_DQS#_1	AM15
M_DQS B N2	AP8	SB_DQS#_2	AR15
M_DQS B N3	AV12	SB_DQS#_3	AL15
M_DQS B N4	AN26	SB_DQS#_4	AM15
M_DQS B N5	AR33	SB_DQS#_5	AP15
M_DQS B N6	AM33	SB_DQS#_6	
M_DQS B N7	AG34	SB_DQS#_7	

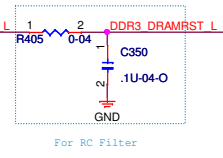
Pay Attention to This Part!

CPU1D

CPU1D			
BALLMAP_REV=1.4			
M_DATA B0	AG7	SB_DQ_0	AK24
M_DATA B1	AG8	SB_DQ_1	AM20
M_DATA B2	AJ9	SB_DQ_2	AM19
M_DATA B3	AJ8	SB_DQ_3	AK18
M_DATA B4	AG5	SB_DQ_4	AP19
M_DATA B5	AG6	SB_DQ_5	AP18
M_DATA B6	AL6	SB_DQ_6	AM18
M_DATA B7	AJ7	SB_DQ_7	AL18
M_DATA B8	AL7	SB_DQ_8	AN18
M_DATA B9	AM7	SB_DQ_9	AY17
M_DATA B10	AM10	SB_DQ_10	AN23
M_DATA B11	AL10	SB_DQ_11	AU17
M_DATA B12	AL6	SB_DQ_12	AT18
M_DATA B13	AL9	SB_DQ_13	AR26
M_DATA B14	AM9	SB_DQ_14	AY16
M_DATA B15	AP7	SB_DQ_15	AV16
M_DATA B16	AP7	SB_DQ_16	
M_DATA B17	AP10	SB_DQ_17	AR25
M_DATA B18	AR10	SB_DQ_18	AK25
M_DATA B19	AP6	SB_DQ_19	AP24
M_DATA B20	AP6	SB_DQ_20	
M_DATA B21	AP6	SB_DQ_21	
M_DATA B22	AP9	SB_DQ_22	AP23
M_DATA B23	AP9	SB_DQ_23	AM24
M_DATA B24	AM12	SB_DQ_24	AW17
M_DATA B25	AM13	SB_DQ_25	
M_DATA B26	AR13	SB_DQ_26	
M_DATA B27	AP13	SB_DQ_27	AN25
M_DATA B28	AL12	SB_DQ_28	AN26
M_DATA B29	AL12	SB_DQ_29	AL25
M_DATA B30	AR12	SB_DQ_30	AT26
M_DATA B31	AP12	SB_DQ_31	
M_DATA B32	AR28	SB_DQ_32	
M_DATA B33	AR29	SB_DQ_33	
M_DATA B34	AL28	SB_DQ_34	AU16
M_DATA B35	AL29	SB_DQ_35	AY15
M_DATA B36	AP28	SB_DQ_36	AW15
M_DATA B37	AP29	SB_DQ_37	AV15
M_DATA B38	AM28	SB_DQ_38	
M_DATA B39	AM29	SB_DQ_39	
M_DATA B40	AP32	SB_DQ_40	
M_DATA B41	AP31	SB_DQ_41	
M_DATA B42	AP35	SB_DQ_42	AL26
M_DATA B43	AP34	SB_DQ_43	AP26
M_DATA B44	AR32	SB_DQ_44	AM26
M_DATA B45	AR31	SB_DQ_45	AK26
M_DATA B46	AR35	SB_DQ_46	
M_DATA B47	AR34	SB_DQ_47	
M_DATA B48	AM32	SB_DQ_48	
M_DATA B49	AM31	SB_DQ_49	
M_DATA B50	AL35	SB_DQ_50	AL21
M_DATA B51	AL32	SB_DQ_51	AL22
M_DATA B52	AM34	SB_DQ_52	AL20
M_DATA B53	AL31	SB_DQ_53	AK20
M_DATA B54	AM35	SB_DQ_54	AL23
M_DATA B55	AL34	SB_DQ_55	AM22
M_DATA B56	AH35	SB_DQ_56	AP21
M_DATA B57	AH34	SB_DQ_57	AN21
M_DATA B58	AE34	SB_DQ_58	
M_DATA B59	AE35	SB_DQ_59	
M_DATA B60	AJ35	SB_DQ_60	
M_DATA B61	AJ34	SB_DQ_61	
M_DATA B62	AF33	SB_DQ_62	
M_DATA B63	AF35	SB_DQ_63	
M_DQS B P0	AH7	SB_DQS_0	AN16
M_DQS B P1	AM8	SB_DQS_1	AN15
M_DQS B P2	AR8	SB_DQS_2	
M_DQS B P3	AN13	SB_DQS_3	
M_DQS B P4	AN29	SB_DQS_4	AL16
M_DQS B P5	AP33	SB_DQS_5	AM16
M_DQS B P6	AL33	SB_DQS_6	AP16
M_DQS B P7	AG35	SB_DQS_7	AR16
M_DQS B N0	AH6	SB_DQS#_0	AL15
M_DQS B N1	AL8	SB_DQS#_1	AM15
M_DQS B N2	AP8	SB_DQS#_2	AR15
M_DQS B N3	AV12	SB_DQS#_3	AL15
M_DQS B N4	AN26	SB_DQS#_4	AM15
M_DQS B N5	AR33	SB_DQS#_5	AP15
M_DQS B N6	AM33	SB_DQS#_6	
M_DQS B N7	AG34	SB_DQS#_7	

SKT\_H2\_CRB

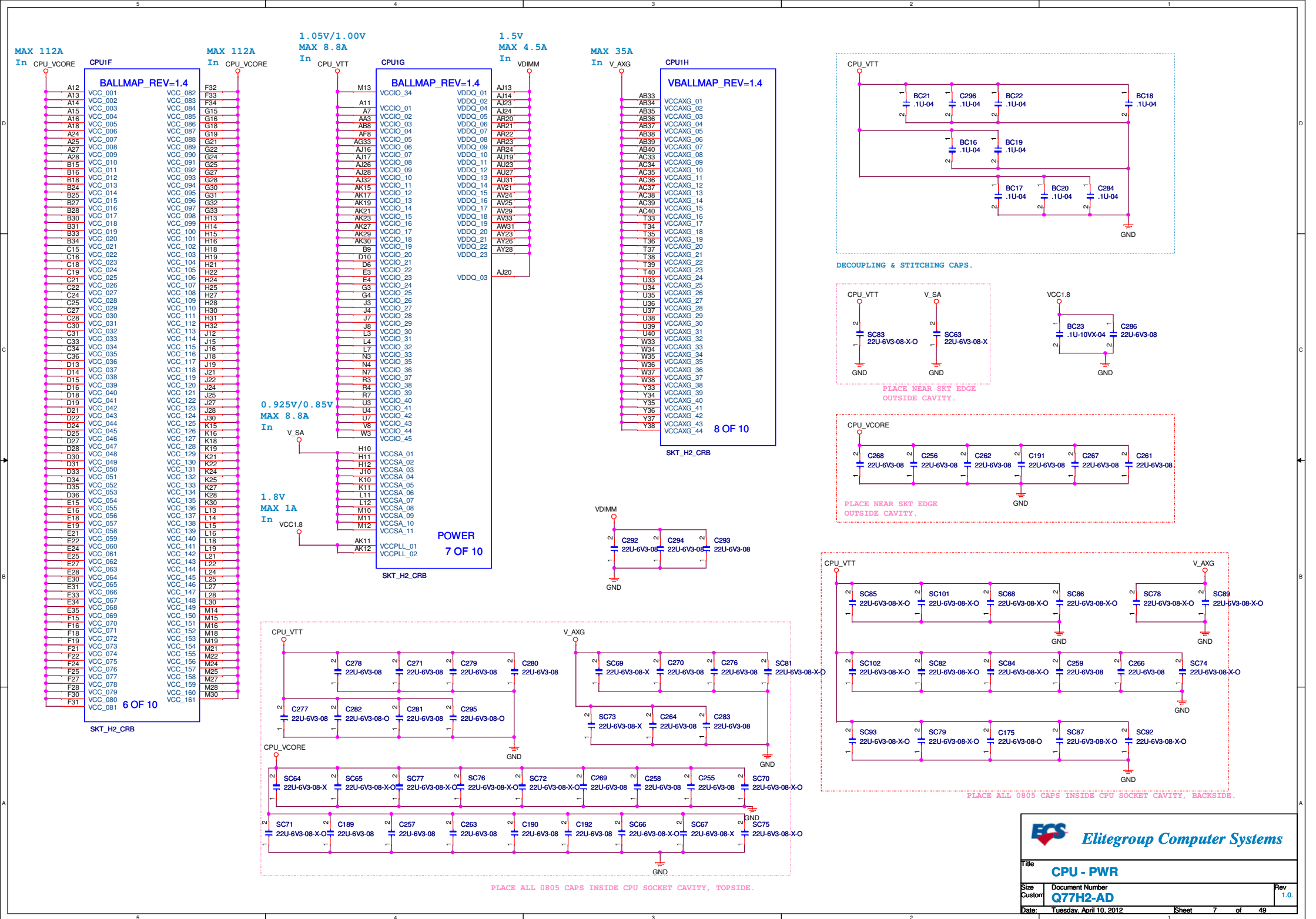
DDR3 CH.B



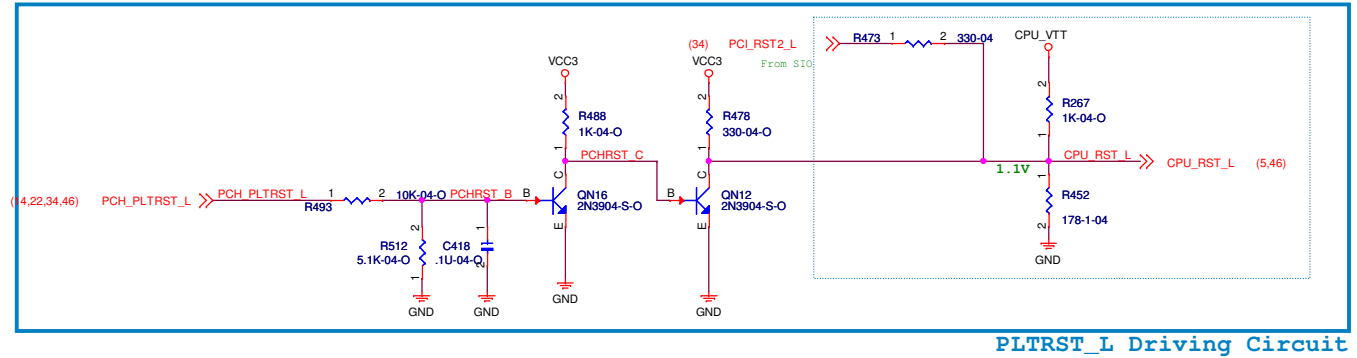
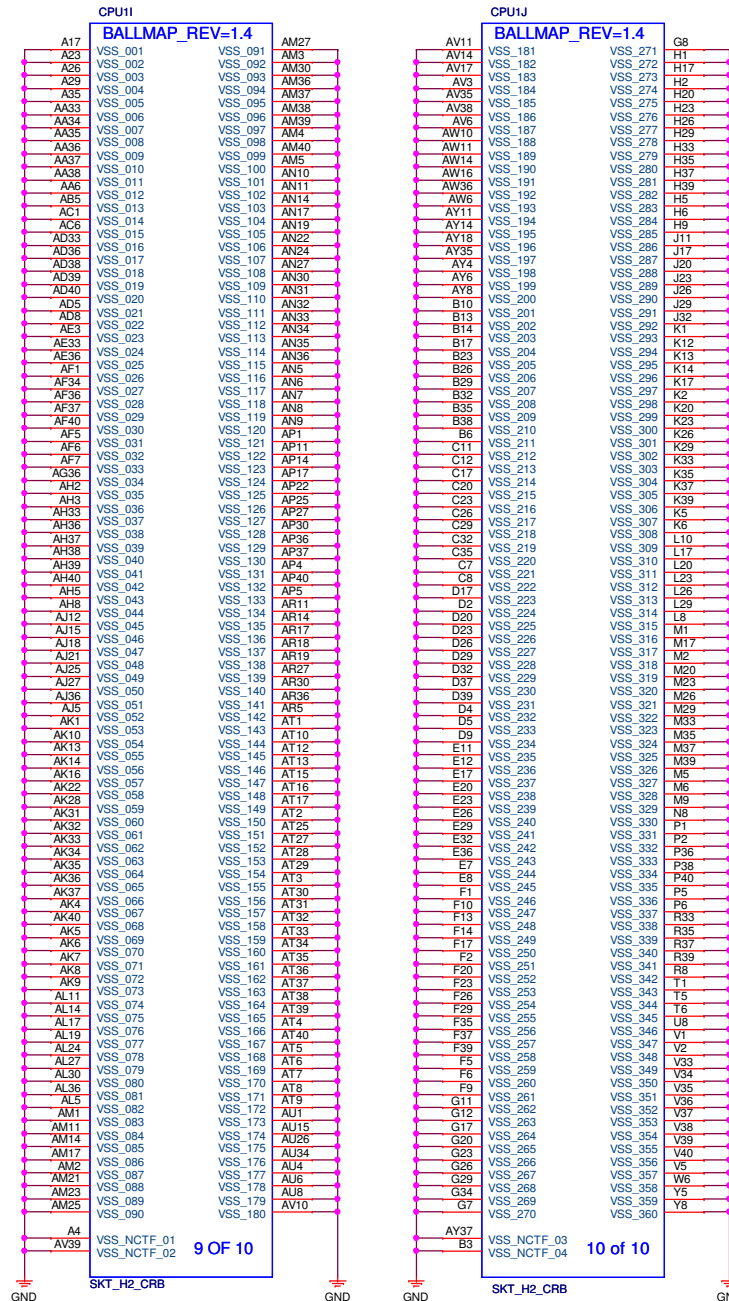
For RC Filter

Desktop dosen't support ECC

Desktop dosen't support ECC



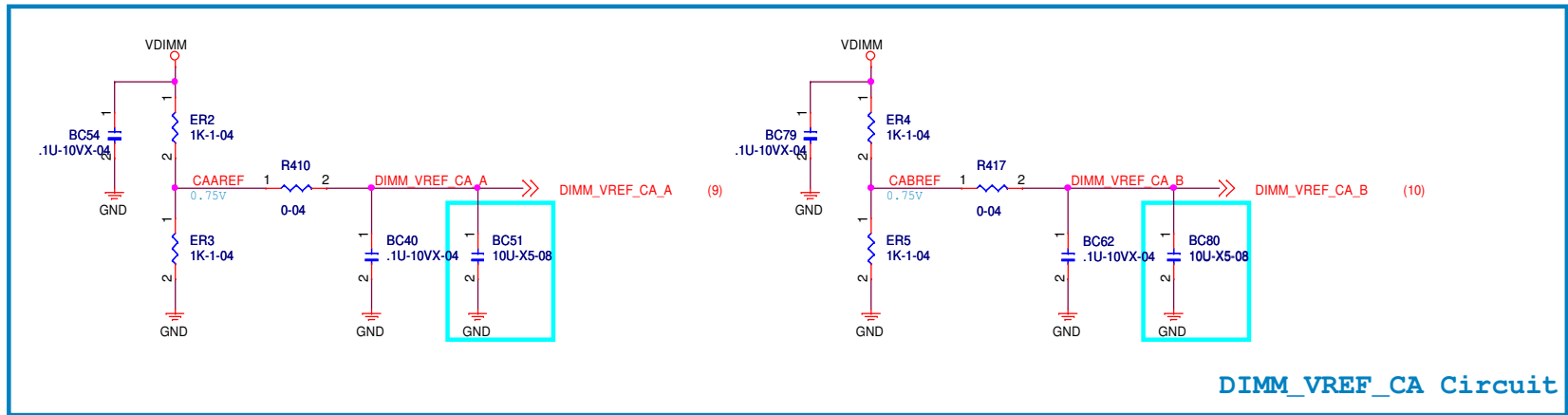
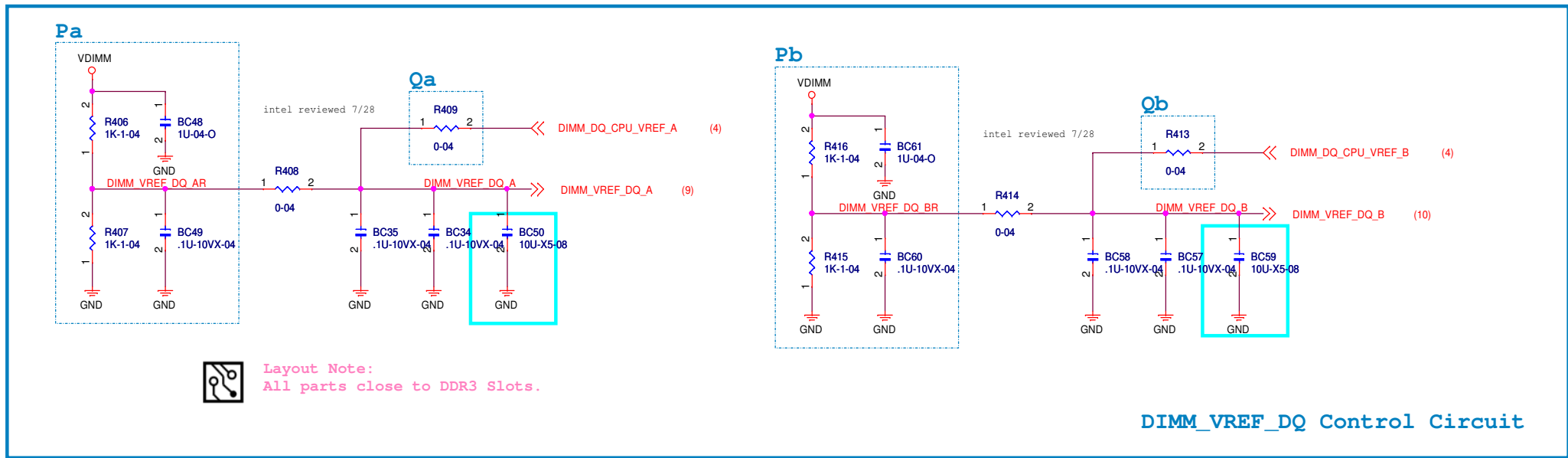




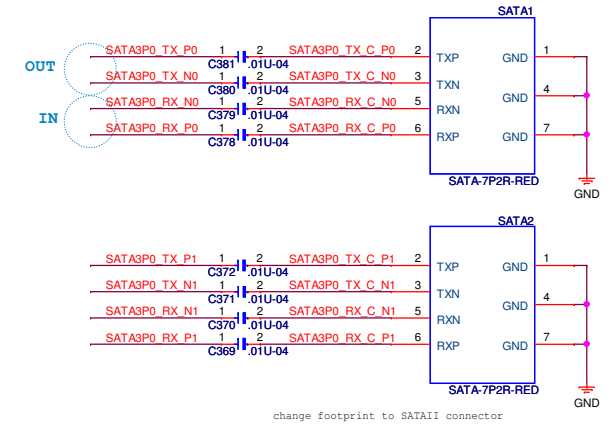
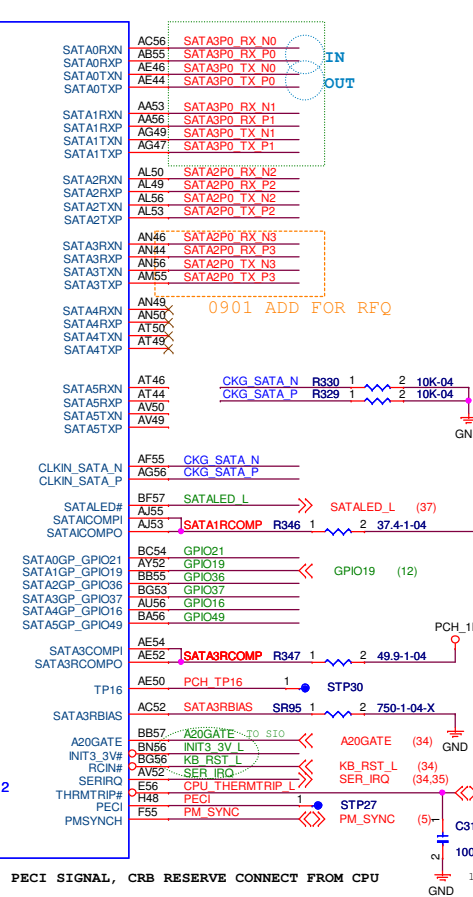
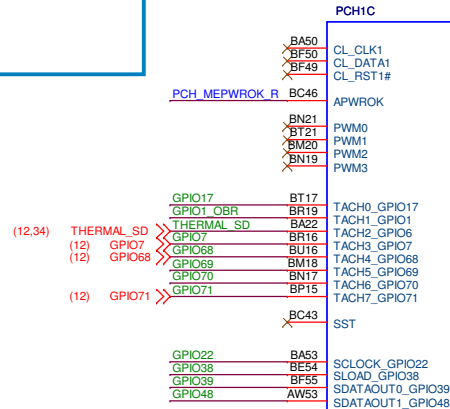
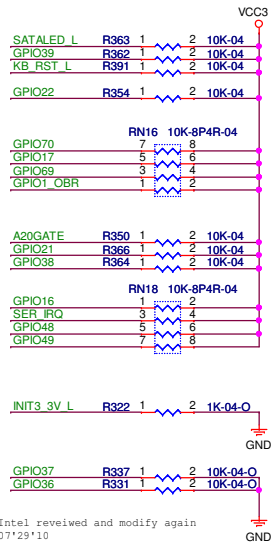
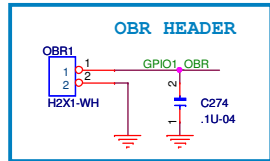
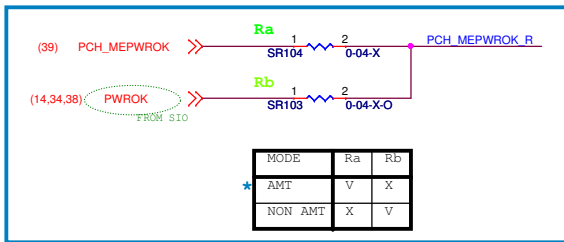








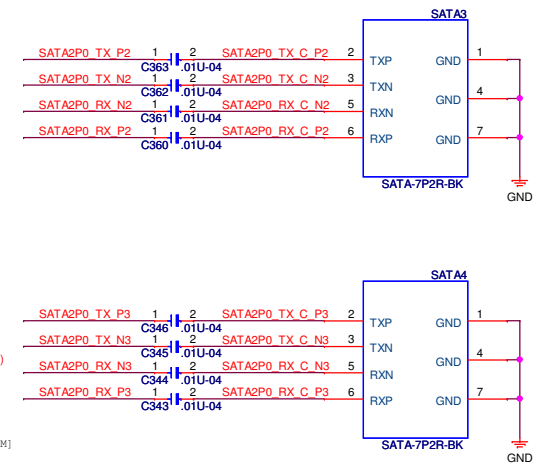


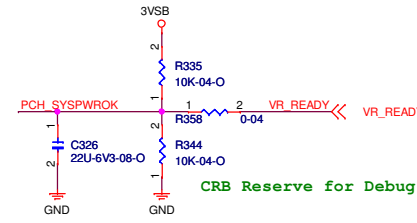
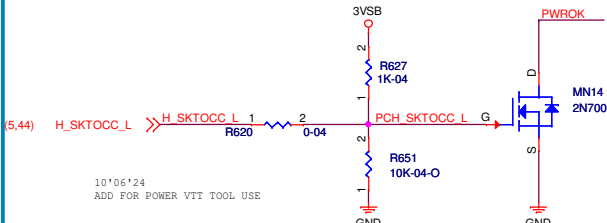
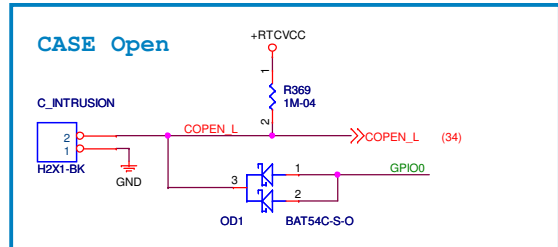
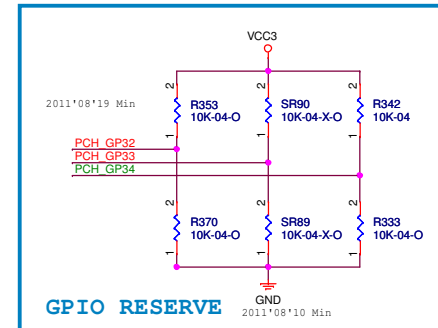
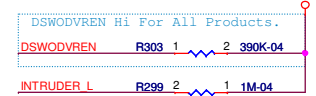
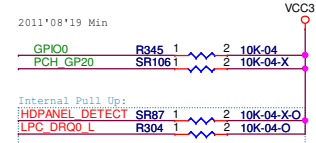
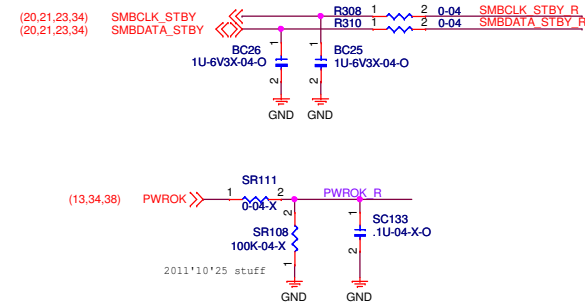
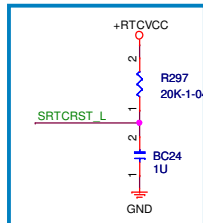
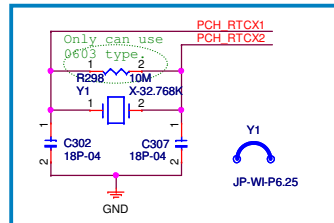
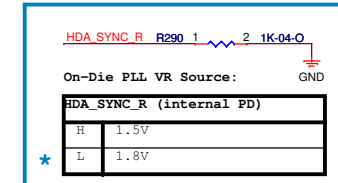
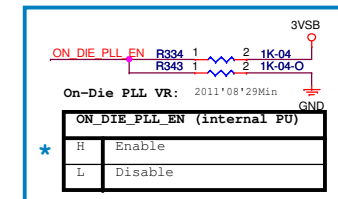
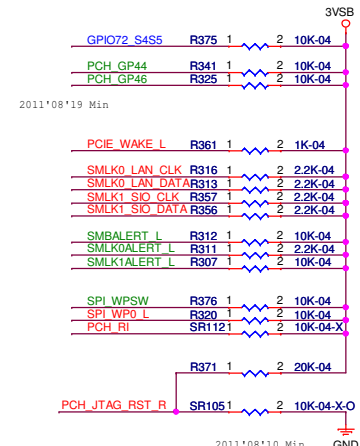
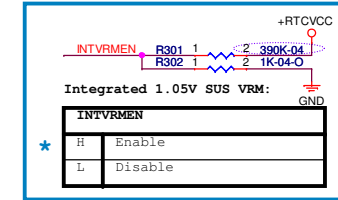
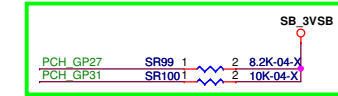
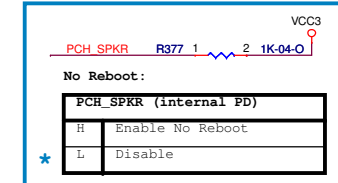
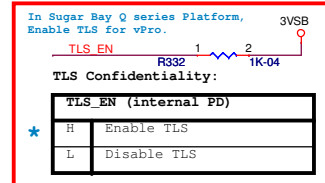
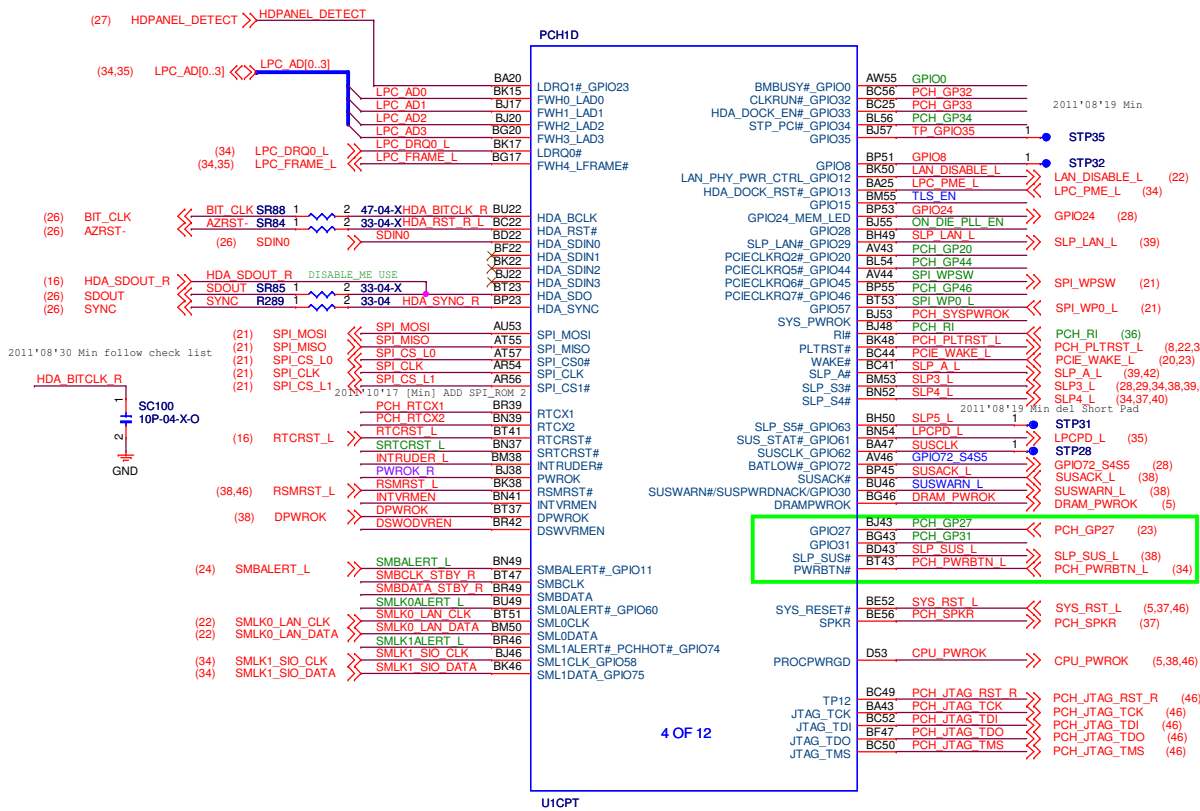


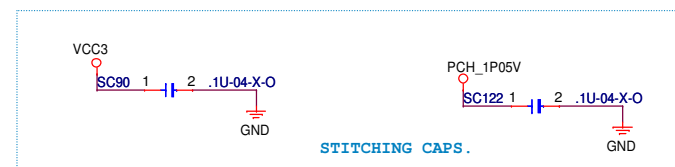
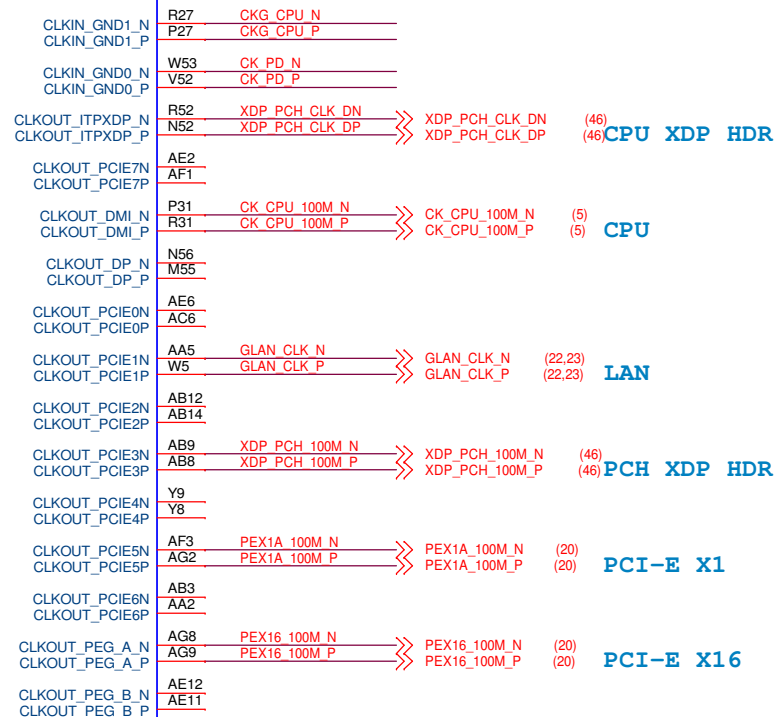
Layout Note:

SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%

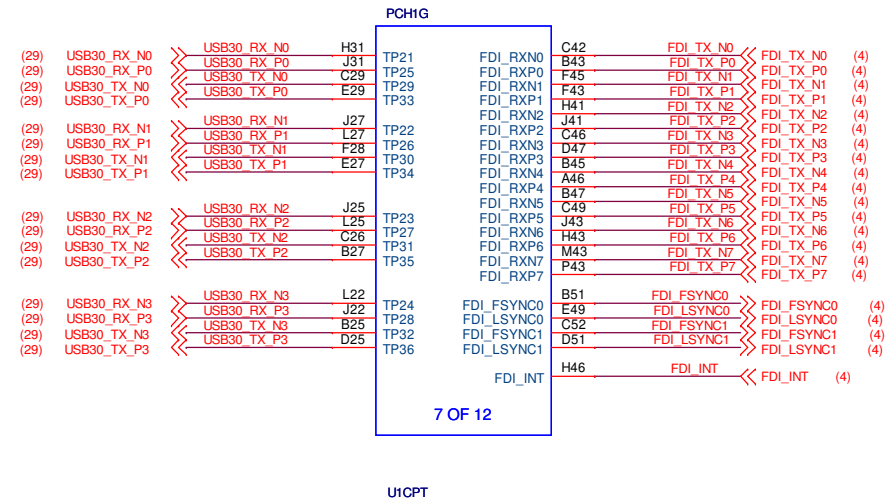
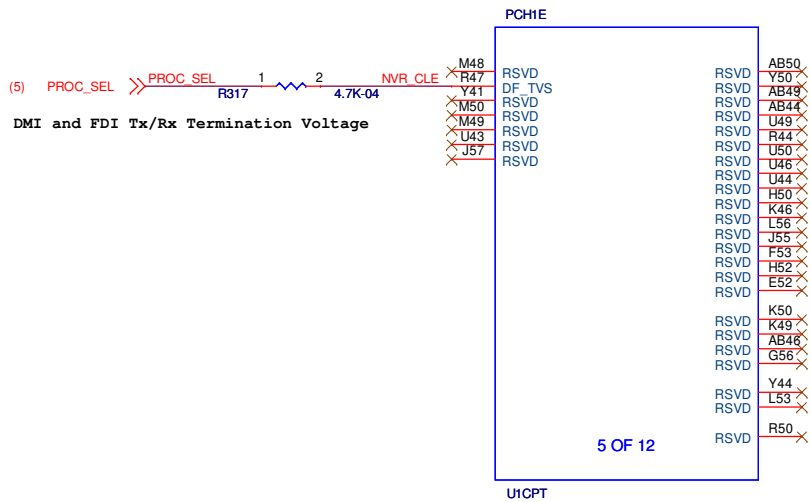
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%



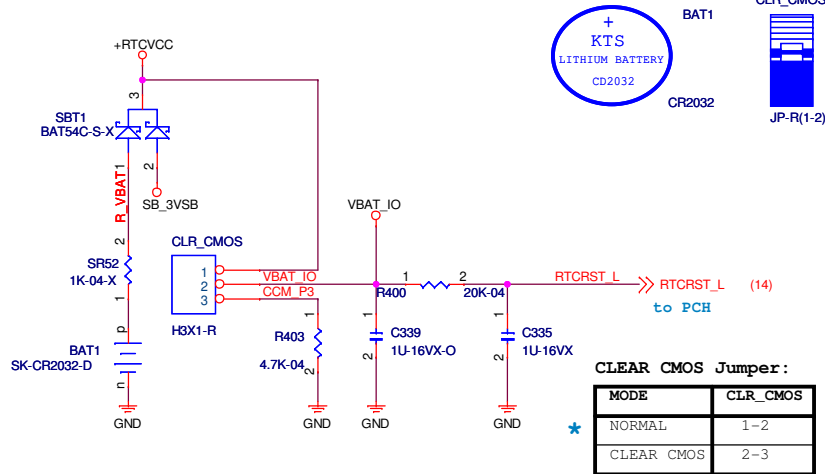




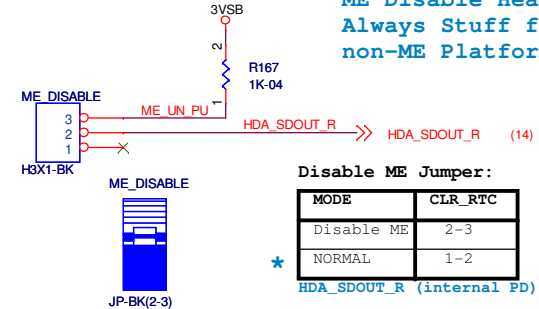




## CLR\_CMOS



ME Disable Header,  
Always Stuff for ME or  
non-ME Platform.



Elitegroup Computer Systems

Title PCH - USB3.0/FDI, CLR\_CMOS

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Port-B: DVII

Port-C: DP

Port-D: DP

[M 1007] PORTB CHANGE TO CONNECT TO DVI-I  
PORT D CHANGE TO CONNECT TO DP

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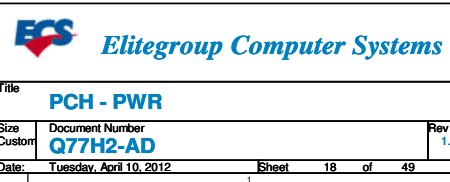
Port C Detected(Internal PD):  
Port C is Detected when High,  
Port C is not Detect when Low.  
Port D Detected(Internal PD):  
Port D is Detected when High,  
Port D is not Detect when Low.  
Port B Detected(Internal PD):  
Port B is Detected when High,  
Port B is not Detect when Low.

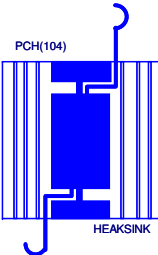
[M 1007] PORTB CHANGE TO CONNECT TO DVI-I  
PORT D CHANGE TO CONNECT TO DP



Elitegroup Computer Systems

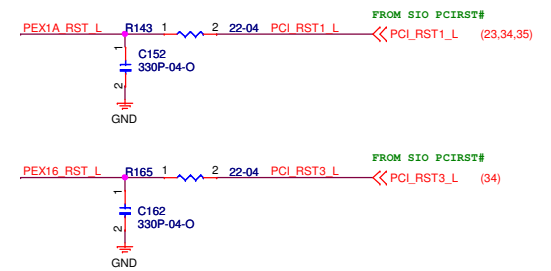
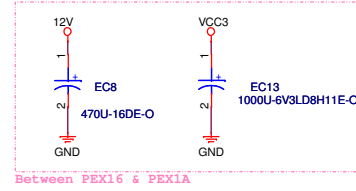
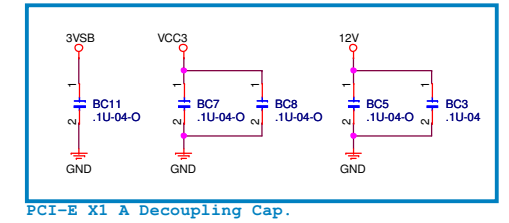
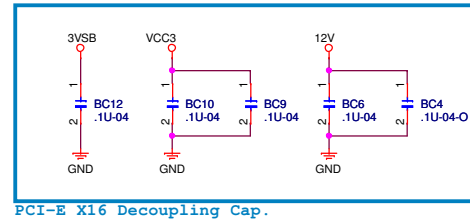
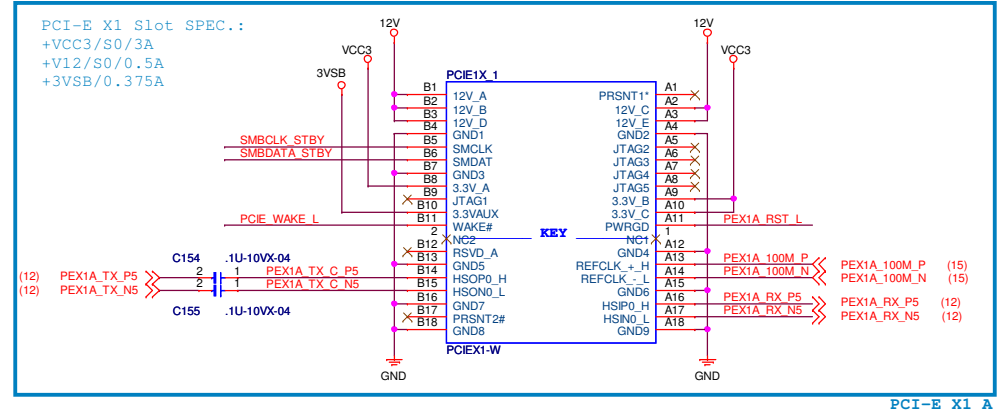
Title <b>PCH - DISPLAY/VGA</b>		
Size Custom	Document Number <b>Q77H2-AD</b>	Rev <b>1.0.</b>
Date: Tuesday, April 10, 2012		Sheet 17 of 49



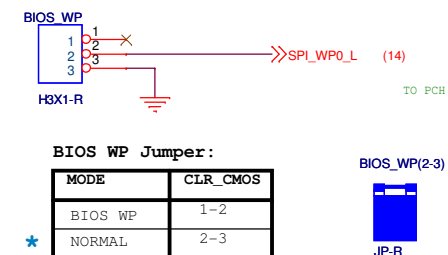
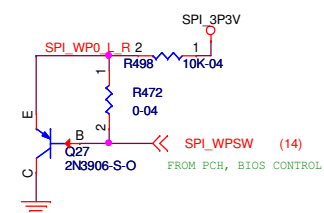
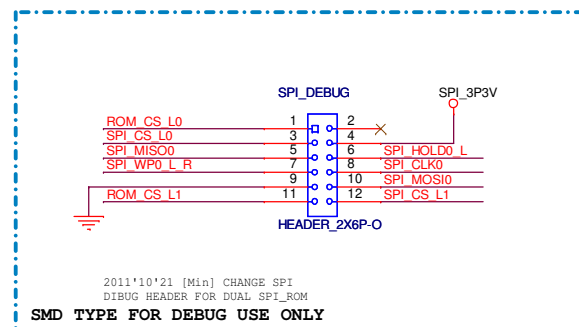
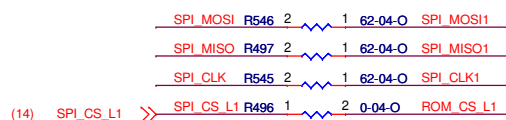
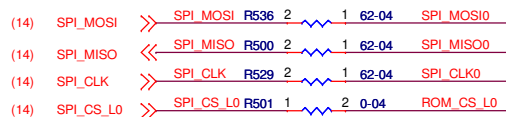
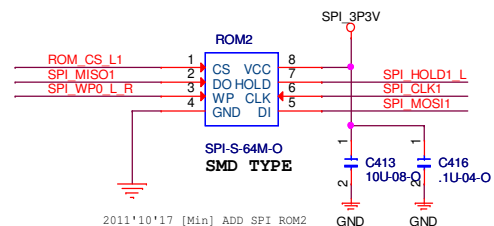
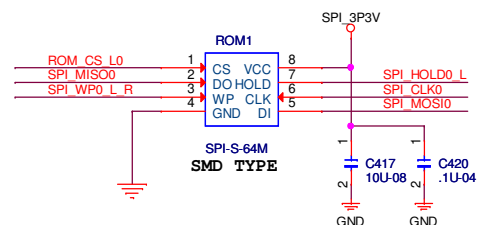
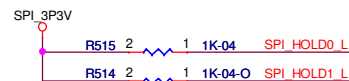
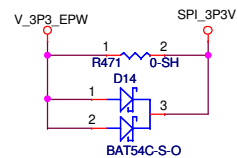


Title			
PCH - GND			
Size	Document Number	Rev	
Custom	Q77H2-AD	1.0	
Date:	Tuesday, April 10, 2012	Sheet	19 of 49

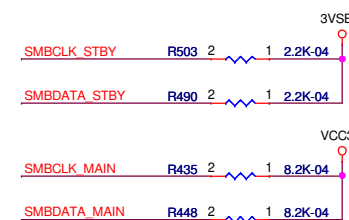
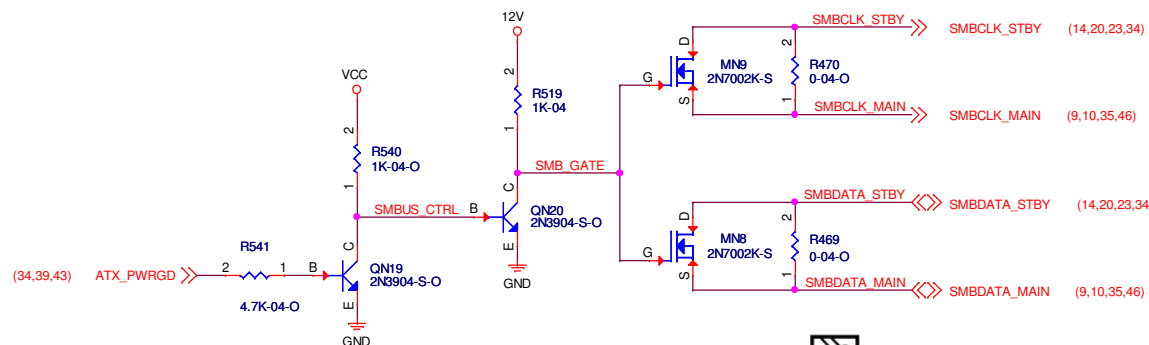
PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A



## SPI ROM Circuit



## SMBUS Logic Circuit



Layout Note:  
SMBUS Trace Max 21500MILS



**Elitegroup Computer Systems**

Title	<b>SPI ROM, SMBUS</b>
-------	-----------------------

Size	Document Number
Custom	<b>Q77H2-AD</b>

Rev	1.0.
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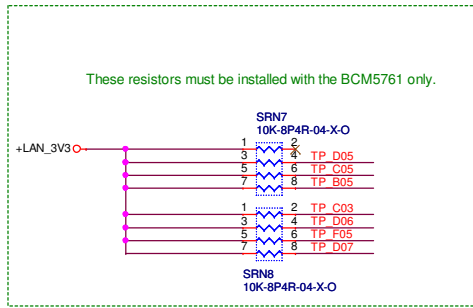
Date: Tuesday, April 10, 2012

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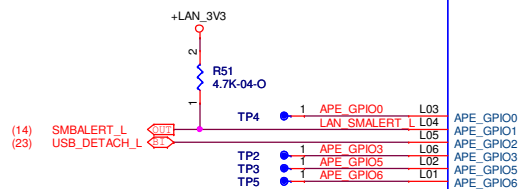




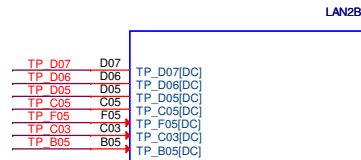
Ruart\_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8\_pd must be installed with the BCM5761 only.

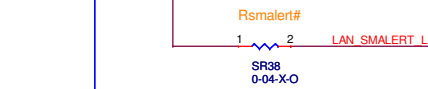
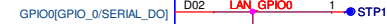
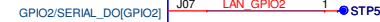
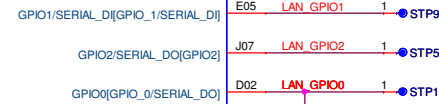


Rvss\_5754 must be installed when the BCM5754 is used.

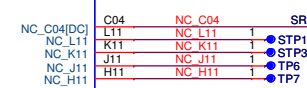


## BCM5761/BCM5754

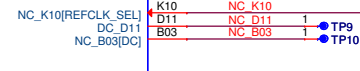
Name - 5761  
Name - 5754 unless different  
[Name] - 5754 only



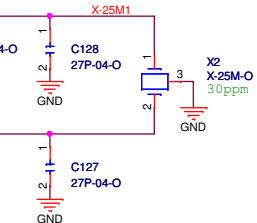
Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.



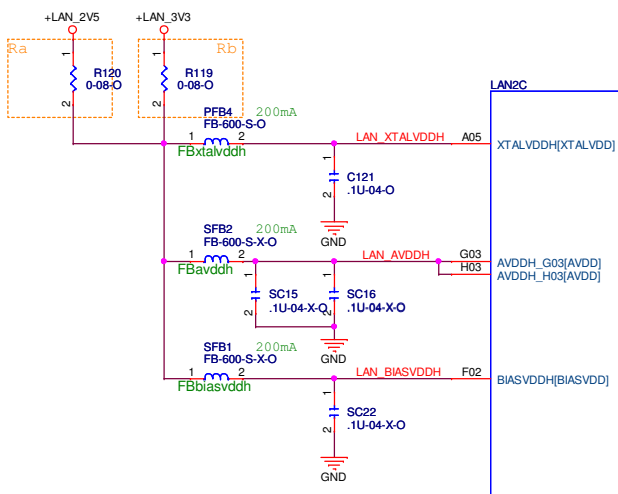
For Energy Detection function use only for 5761E use



Rrefcksel must not be installed with the BCM5761, but may be installed with the BCM5754



	5754	5761
Ra	V	X
Rb	X	V



### BCM5761/BCM5754

Name - 5761  
Name - 5754 unless different  
[Name] - 5754 only

VDDIO\_K08  
VDDIO\_H10  
VDDIO\_C02  
VDDIO\_A03

VDDC\_H08  
VDDC\_G09  
VDDC\_G08  
VDDC\_E10  
VDDC\_C09

REGCTL12

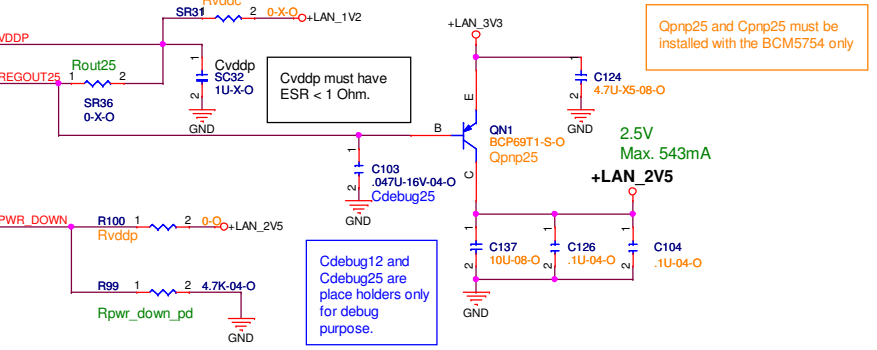
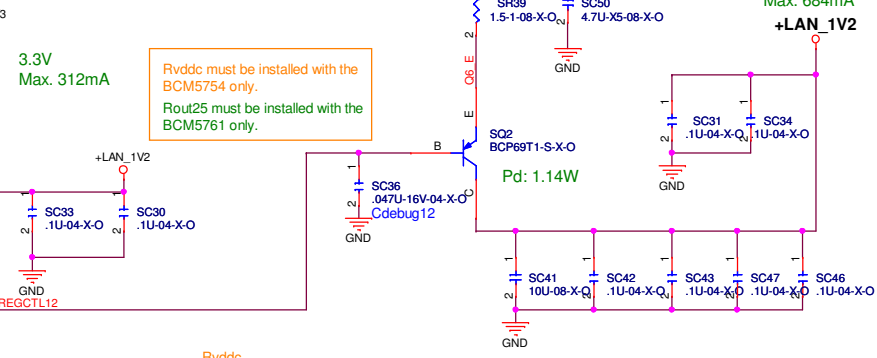
VDDP[VDDC]

REGOUT25[REGCTL25]

PWR\_DOWN[VDDP]

H09  
VSS\_H04  
VSS\_G11  
VSS\_G06  
VSS\_G04  
VSS\_F08  
VSS\_F07  
VSS\_F06  
VSS\_E08  
VSS\_E07  
VSS\_E06  
VSS\_E04  
VSS\_D04  
VSS\_D03  
VSS\_D06  
VSS\_B11  
VSS\_B07  
VSS\_A11  
VSS\_A09  
VSS\_A07  
VSS\_A02

GND



Rvddp must be installed with the BCM5754 only.  
Rpwr\_down\_pd must be installed with the BCM5761 only.  
The PWR\_DWN[VDDP] ball must not be driven to 3.3V. Refer to the BCM5761 data sheet for logic thresholds and maximum ratings.

If the BCM5761 is installed, FBusb\_pll, Cusb\_bulk, and Cusb\_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, FBusb\_pll, Cusb\_bulk, and Cusb\_hf may be uninstalled.

**Elitegroup Computer Systems**

Title

**LAN (BCM5761) PWR & GND**

Size Custom

Document Number

**Q77H2-AD**

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Rev 1.0.

**Depop schematic**

VCC3

R60 10K-04

Q16 FMBT3906-H-S

Q15 FMBT3906-H-S

Q14 FMBT3906-H-S

Q22 FMBT3906-H-S

C145 22uF-6V3-08

R140 10K-04

R142 220K-04

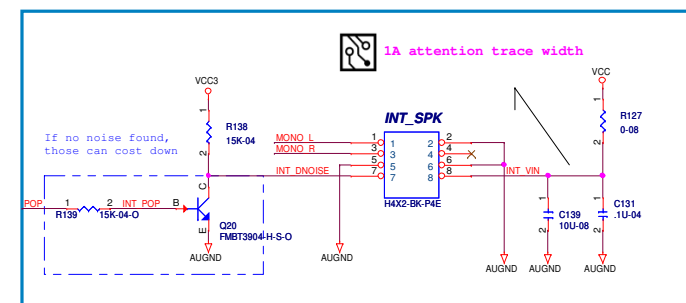
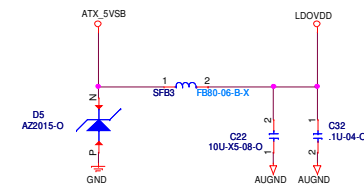
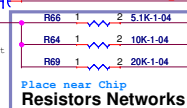
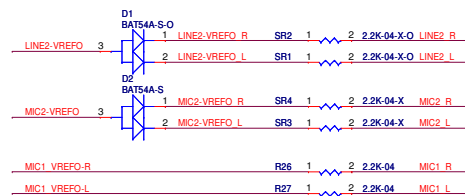
AZRST\_ANTI POP\_ 1K-04 2 1 R96 AZRST\_R 1K-04 2 1 R61 ANTI POP\_R

POP 3

POP 2

POP 1

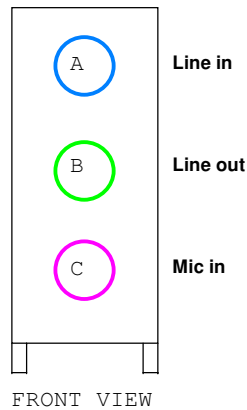
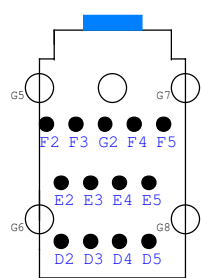
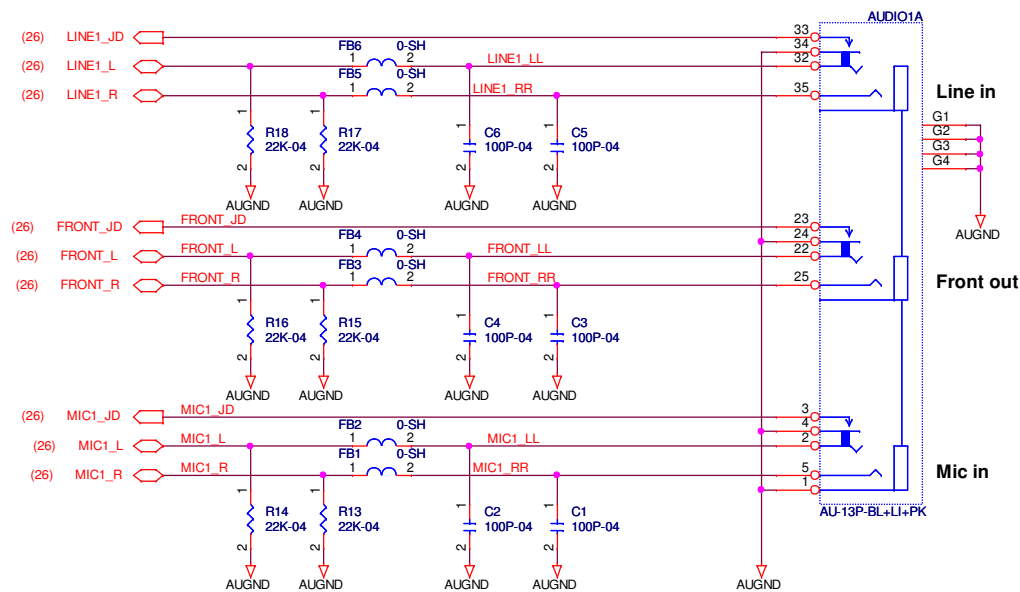
3VSB



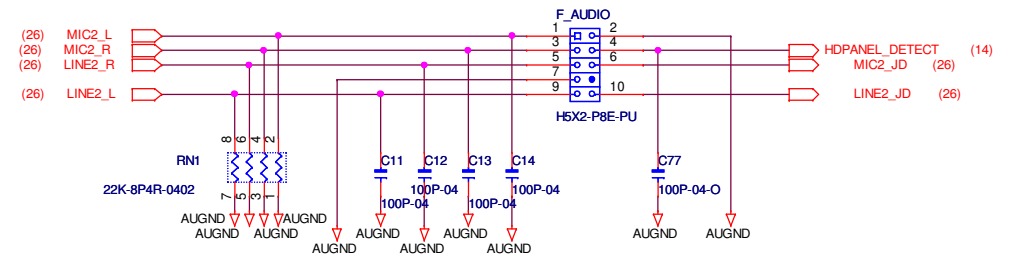
**Elitegroup Computer Systems**

Title			
AUDIO ALC662 (CHIP)			
Size	Document Number	Rev	
Custom	Q77H2-AD	1.0.	
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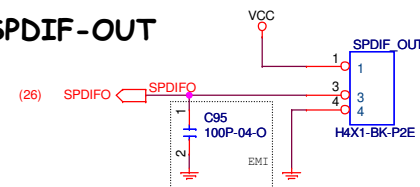
## REAR-AUDIO



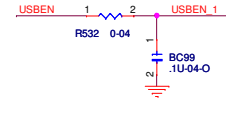
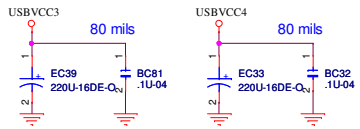
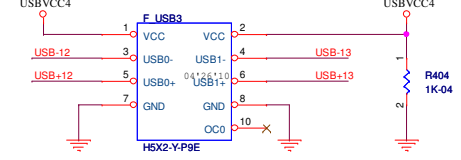
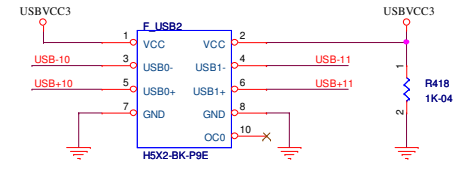
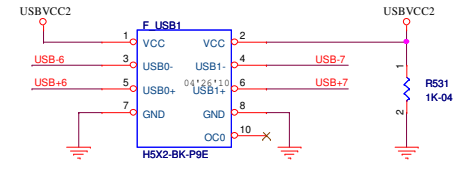
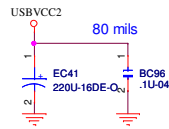
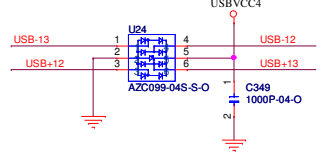
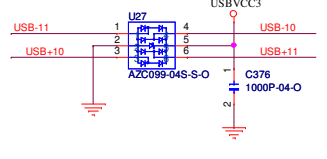
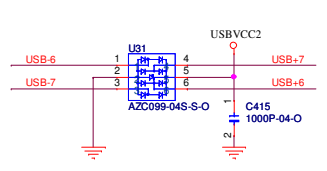
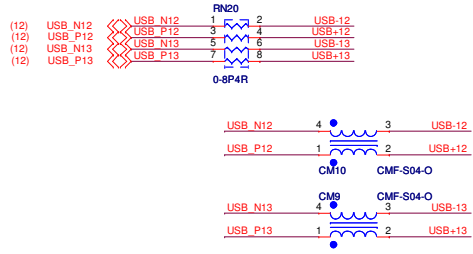
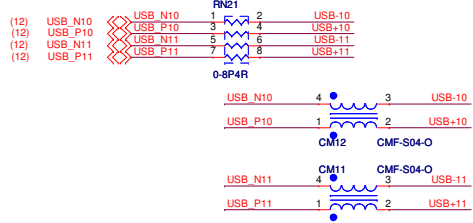
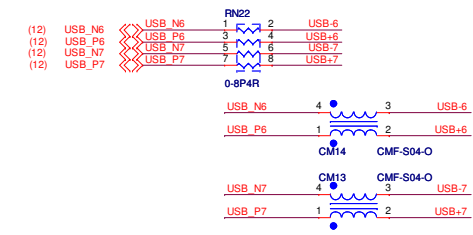
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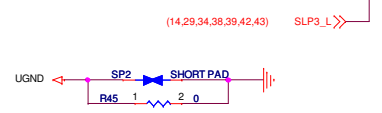
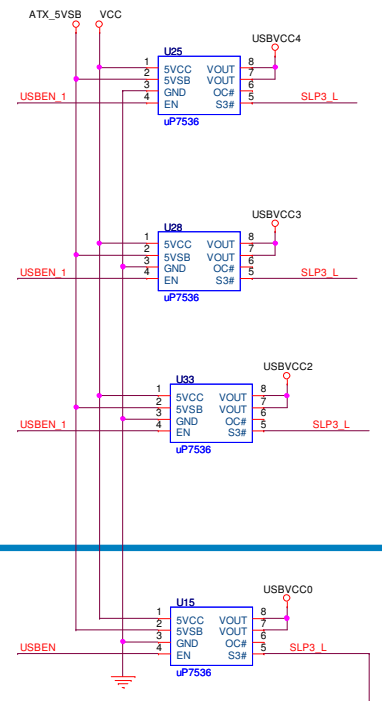
## SPDIF-OUT



<b>AUDIO ALC662 Connector (PANEL)</b>	
Title	Document Number
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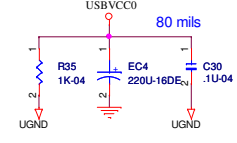
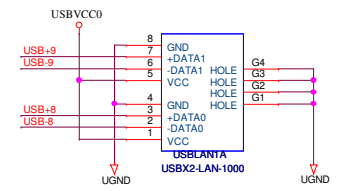
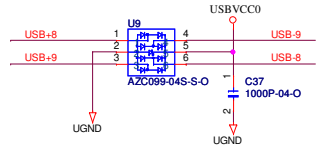
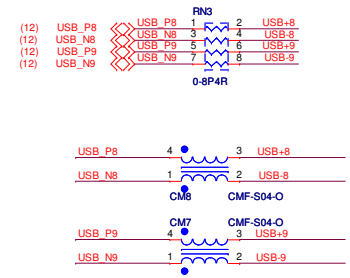


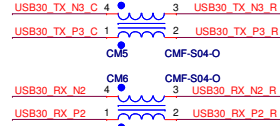
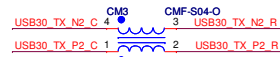
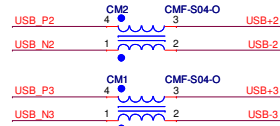
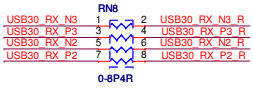
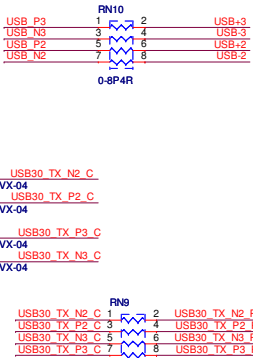
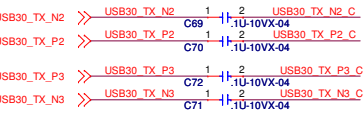
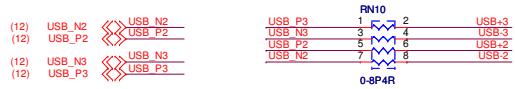
	uP7536 Enable use	Ra	Rb	Rb	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm	N A	N A	0 Volt	Acer CONSUMER
*	PCH GPIO72 default High	N A	100ohm	N A	BIOS CONTROL	Acer COMMERCIAL
	PCH GPIO24 default Low	N A	N A	100ohm	BIOS CONTROL	Acer COMMERCIAL



## FRONT PANEL USB2.0 HEADER

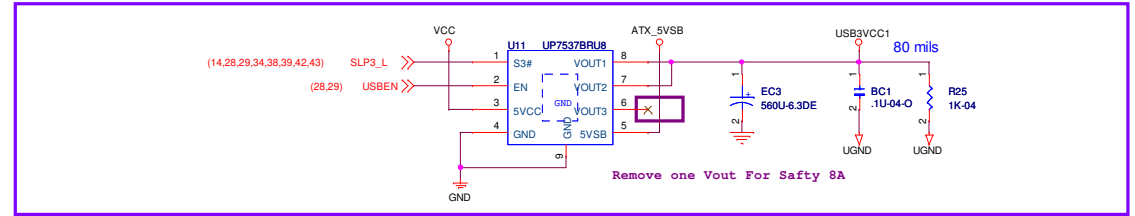
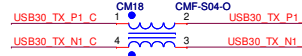
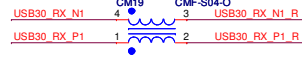
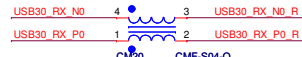
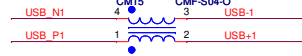
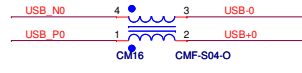
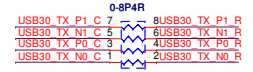
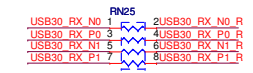
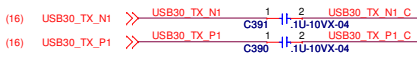
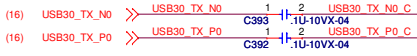
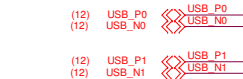
## REAR PANEL USB2.0 CONNECTOR



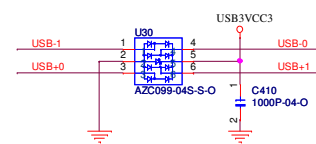
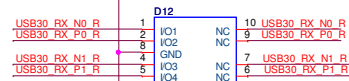
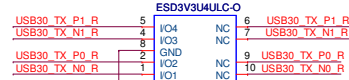
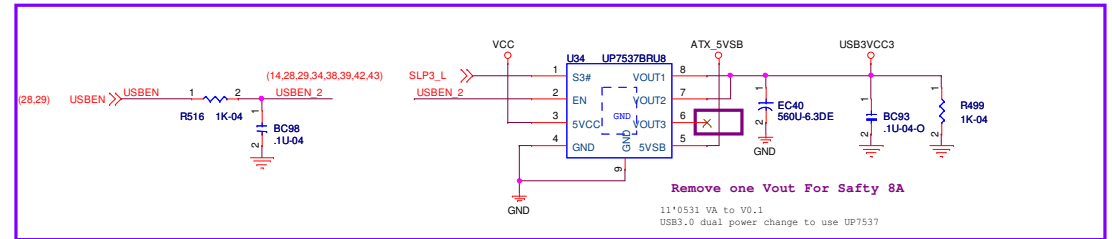
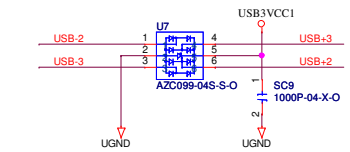
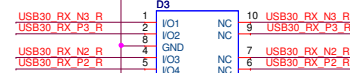
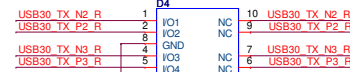


## REAR PANEL USB3.0 CONNECTOR

## FRONT PANEL USB3.0 HEADER

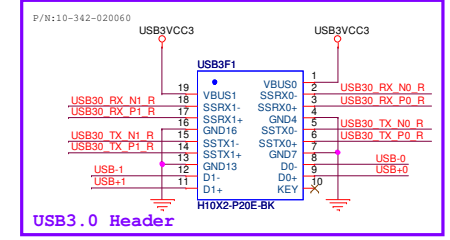
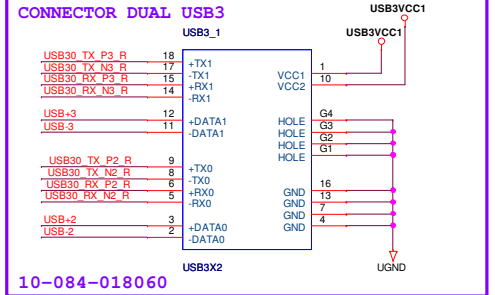


## USB3 ESD COMPONENTS



## USB3 ESD COMPONENTS

NOTE: Port1,Port2 SWAP between Port3, Port4  
2011'03'11



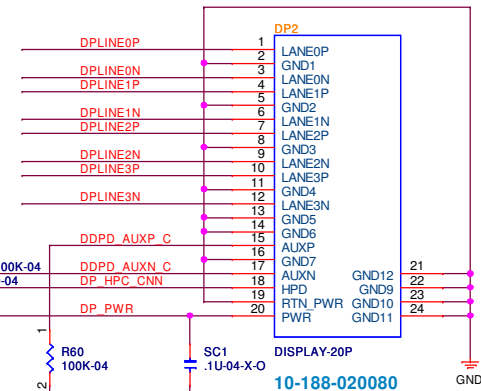
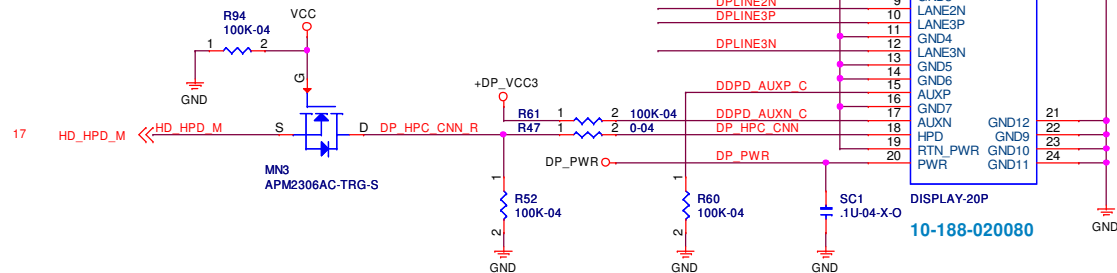
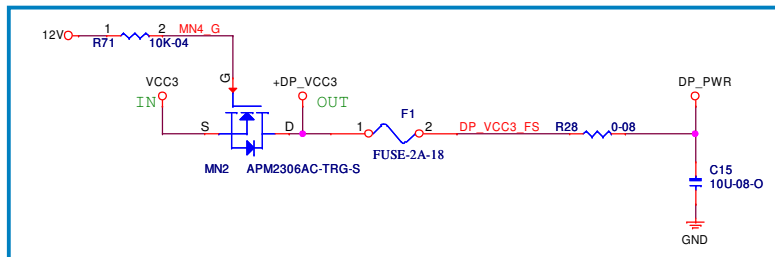




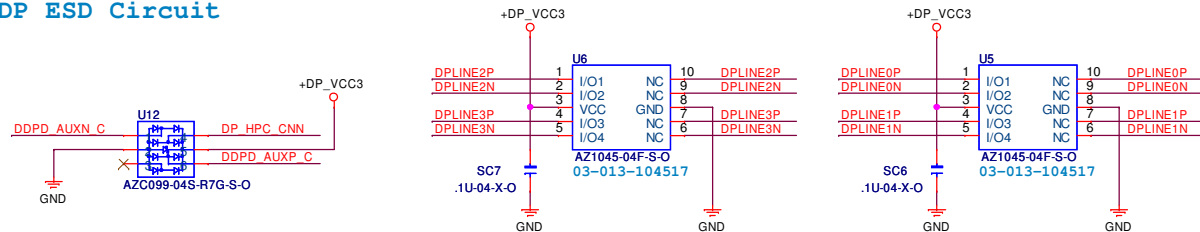
DDPD\_AUXP >> DDPD\_AUXP C80 >> 1U-10VX-04 DDPD\_AUXP C  
DDPD\_AUXN >> DDPD\_AUXN C79 >> 1U-10VX-04 DDPD\_AUXN C

DDPD\_0P >> DDPD\_0P C61 >> 1U-10VX-04 DPLINE0P C 8 7 DPLINE0P  
DDPD\_0N >> DDPD\_0N C62 >> 1U-10VX-04 DPLINE0N C 6 5 DPLINE0N  
DDPD\_1P >> DDPD\_1P C63 >> 1U-10VX-04 DPLINE1P C 4 3 DPLINE1P  
DDPD\_1N >> DDPD\_1N C64 >> 1U-10VX-04 DPLINE1N C 2 1 DPLINE1N  
RN6

DDPD\_2P >> DDPD\_2P C65 >> 1U-10VX-04 DPLINE2P C 8 7 DPLINE2P  
DDPD\_2N >> DDPD\_2N C66 >> 1U-10VX-04 DPLINE2N C 6 5 DPLINE2N  
DDPD\_3P >> DDPD\_3P C67 >> 1U-10VX-04 DPLINE3P C 4 3 DPLINE3P  
DDPD\_3N >> DDPD\_3N C68 >> 1U-10VX-04 DPLINE3N C 2 1 DPLINE3N  
RN7



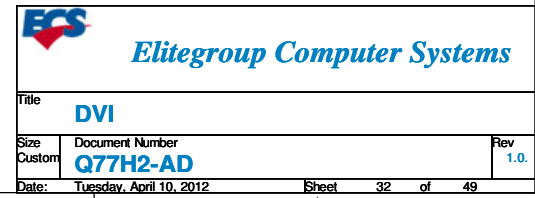
## DP ESD Circuit

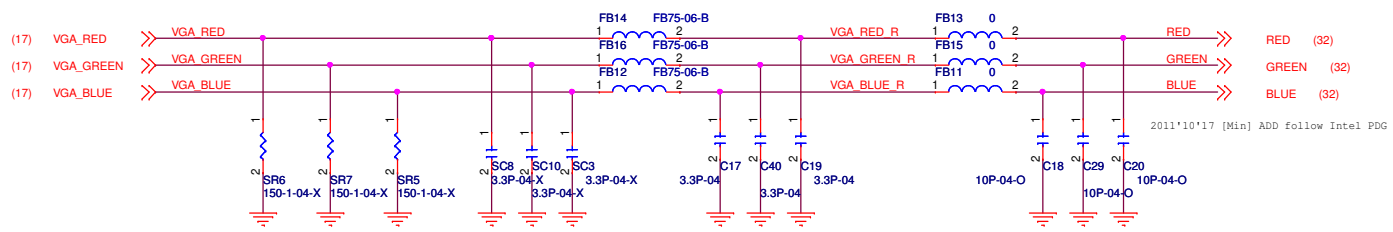


## DISPLAY PORT2

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SU1	ASM1442-X
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**Close to Connector**

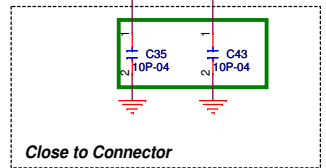


**Close To GMCH**

match the trace impedance.

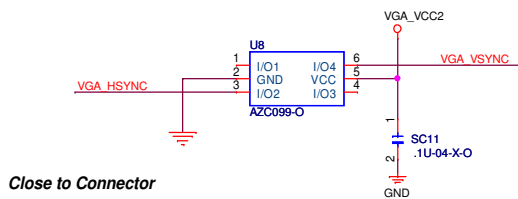
VGA\_HSYNC << VGA\_HSYNC (17,32)

VGA\_VSYNC << VGA\_VSYNC (17,32)



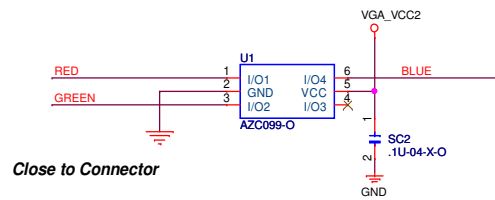
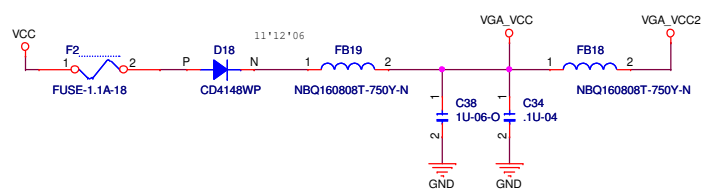
**Close to Connector**

Slew Rate Control

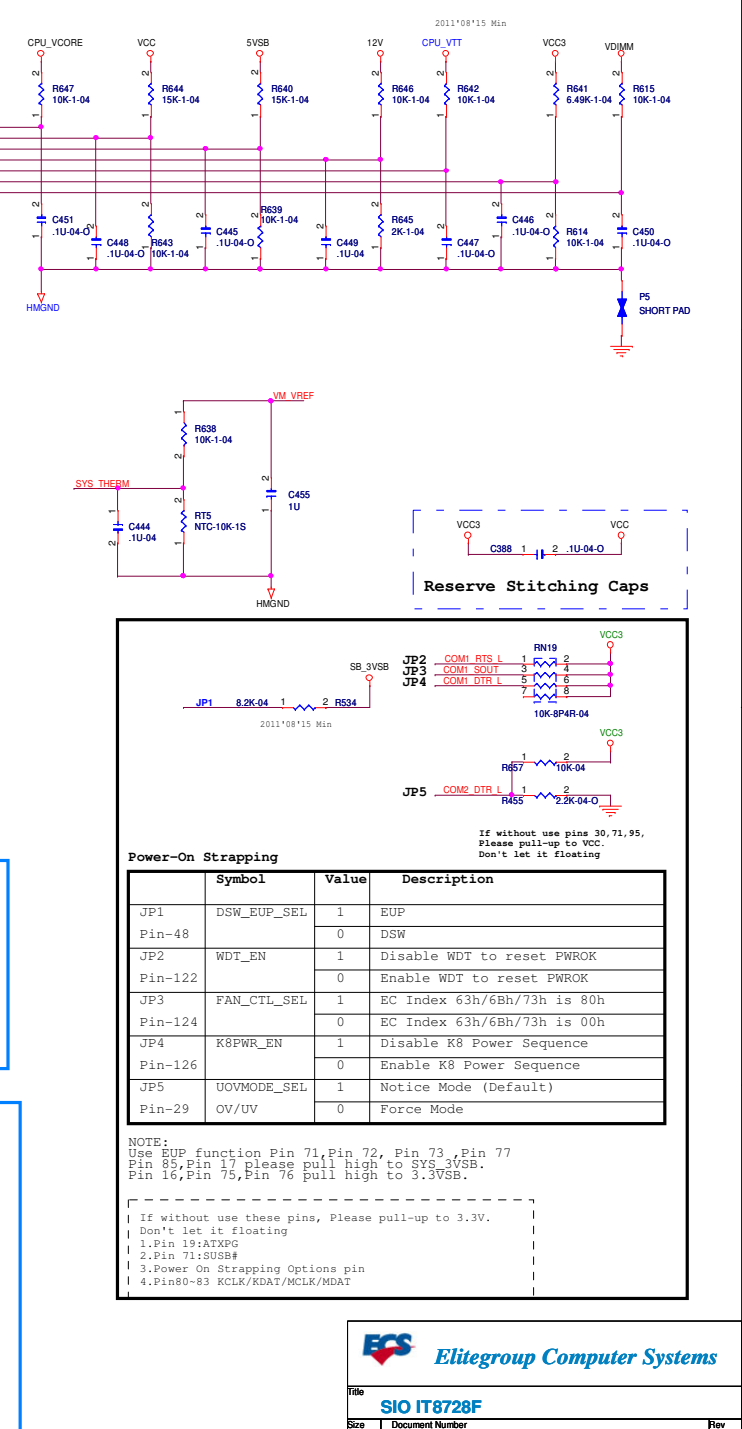


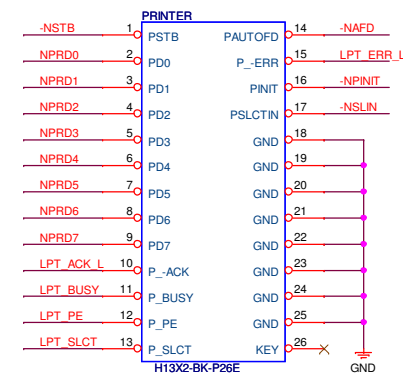
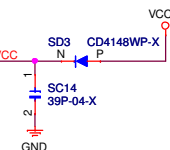
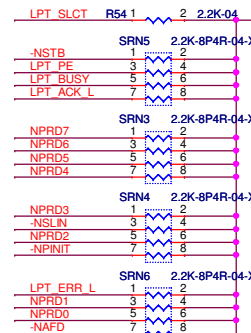
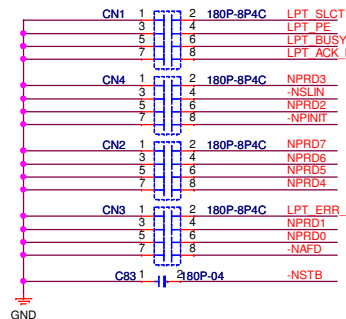
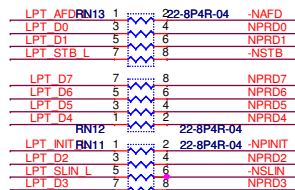
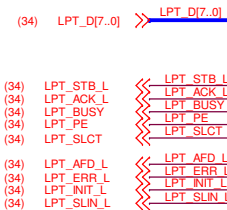
**Close to Connector**

If build in Internal DVI Con,  
that can use the circuit to protect reverse voltage together.



**Close to Connector**

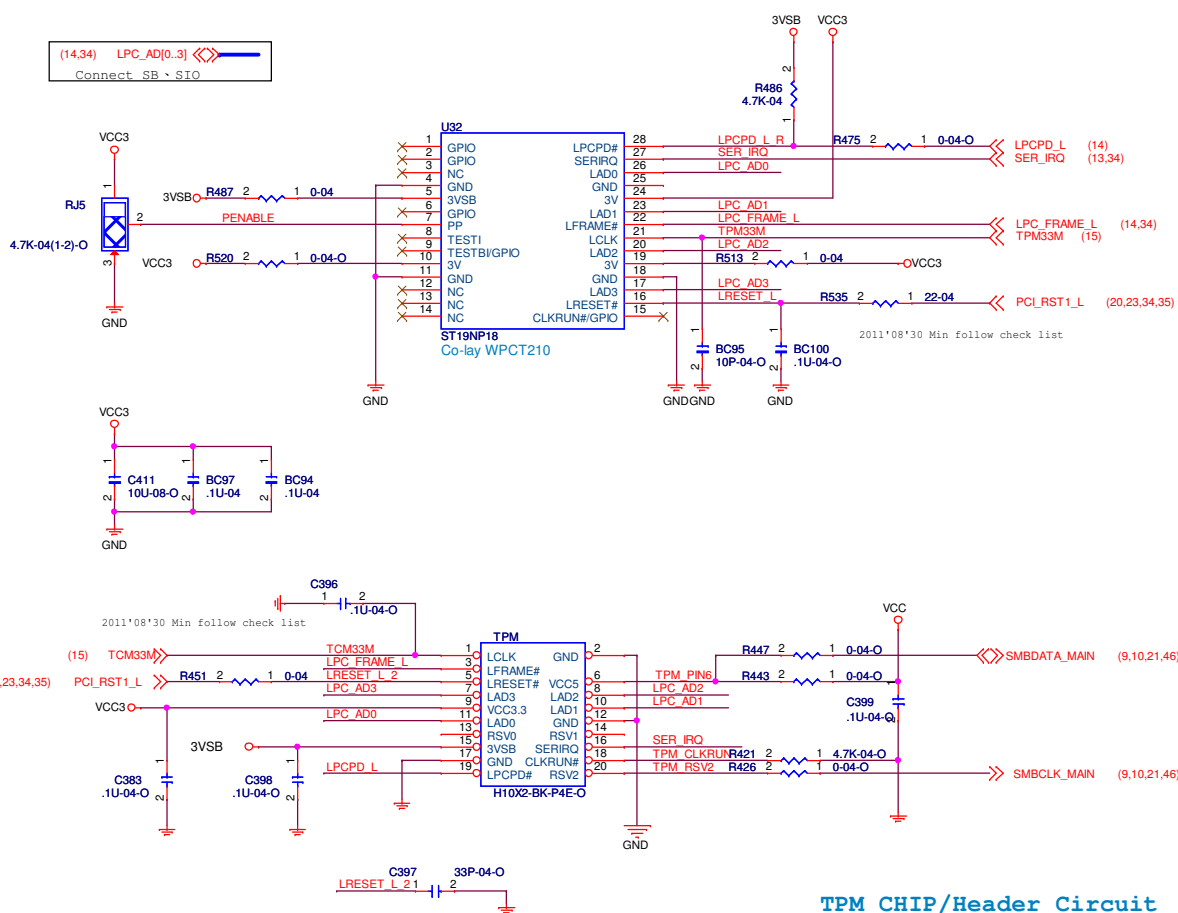


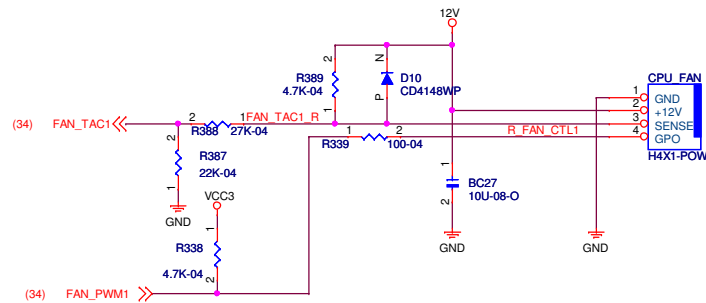


0901 CHANGE FOR RFQ

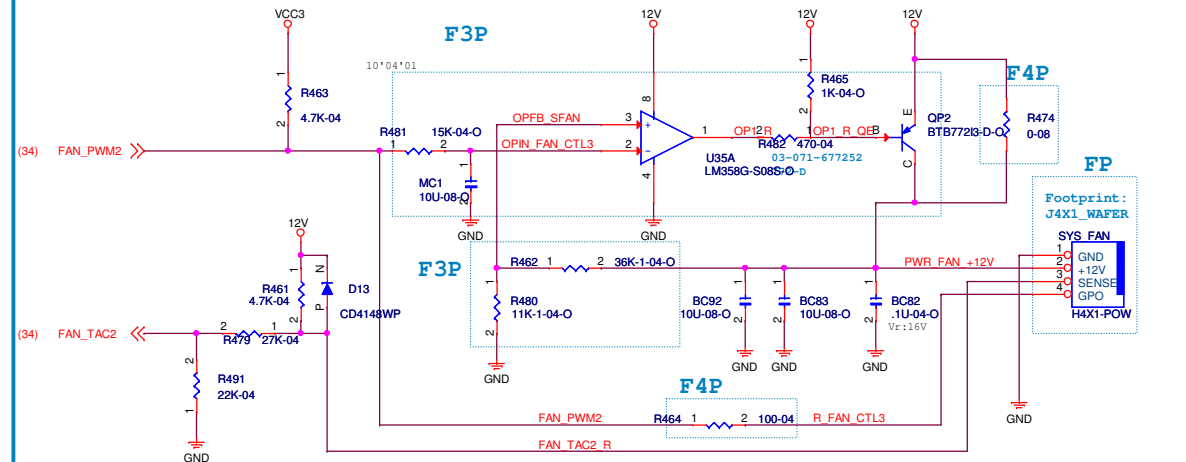
LPT Header Circuit

(14,34) LPC\_AD[0..3] >> Connect\_SB + SIO



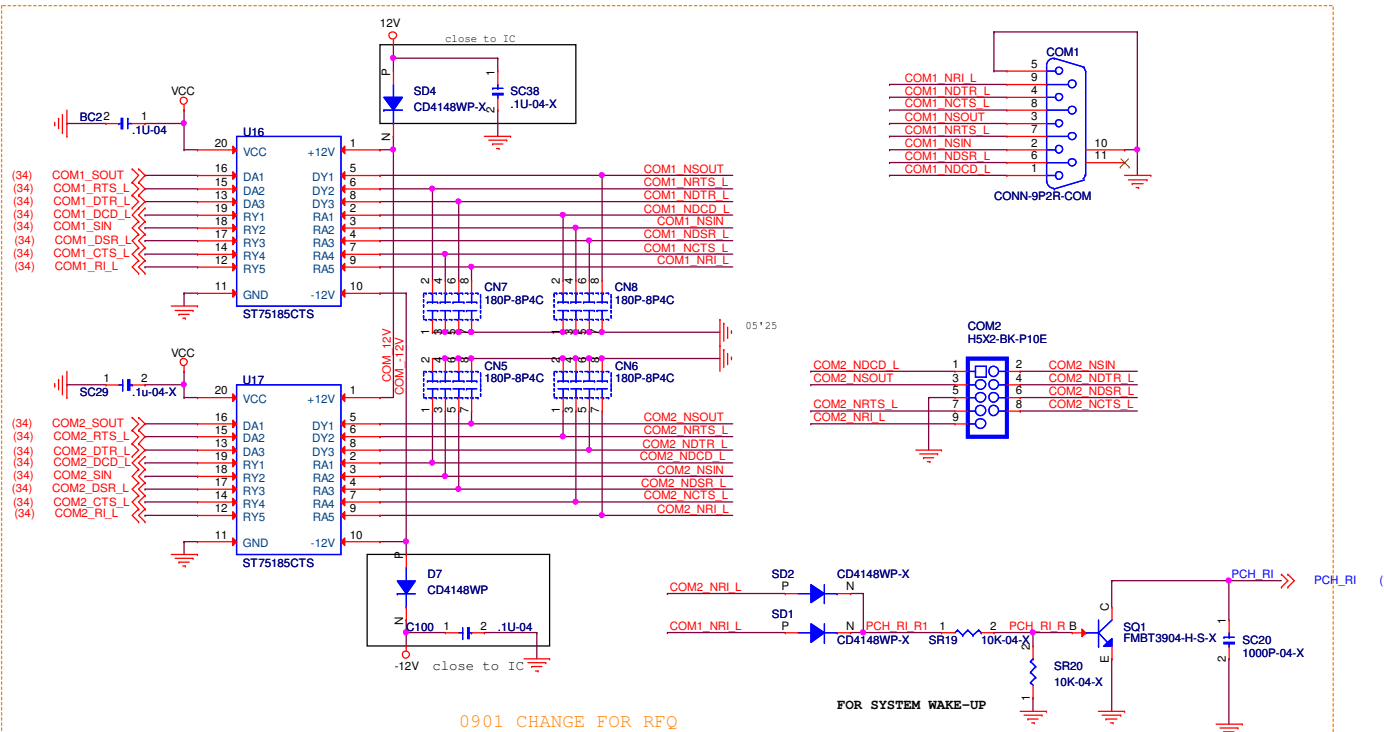


CPU FAN 4-PIN Circuit

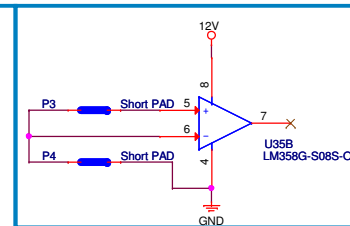


SYS FAN 3-PIN (Co-Lay 4PIN) Circuit

## COM PORT I/O



0901 CHANGE FOR RFQ



PWR FAN:

MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

0901 CHANGE FOR RFQ

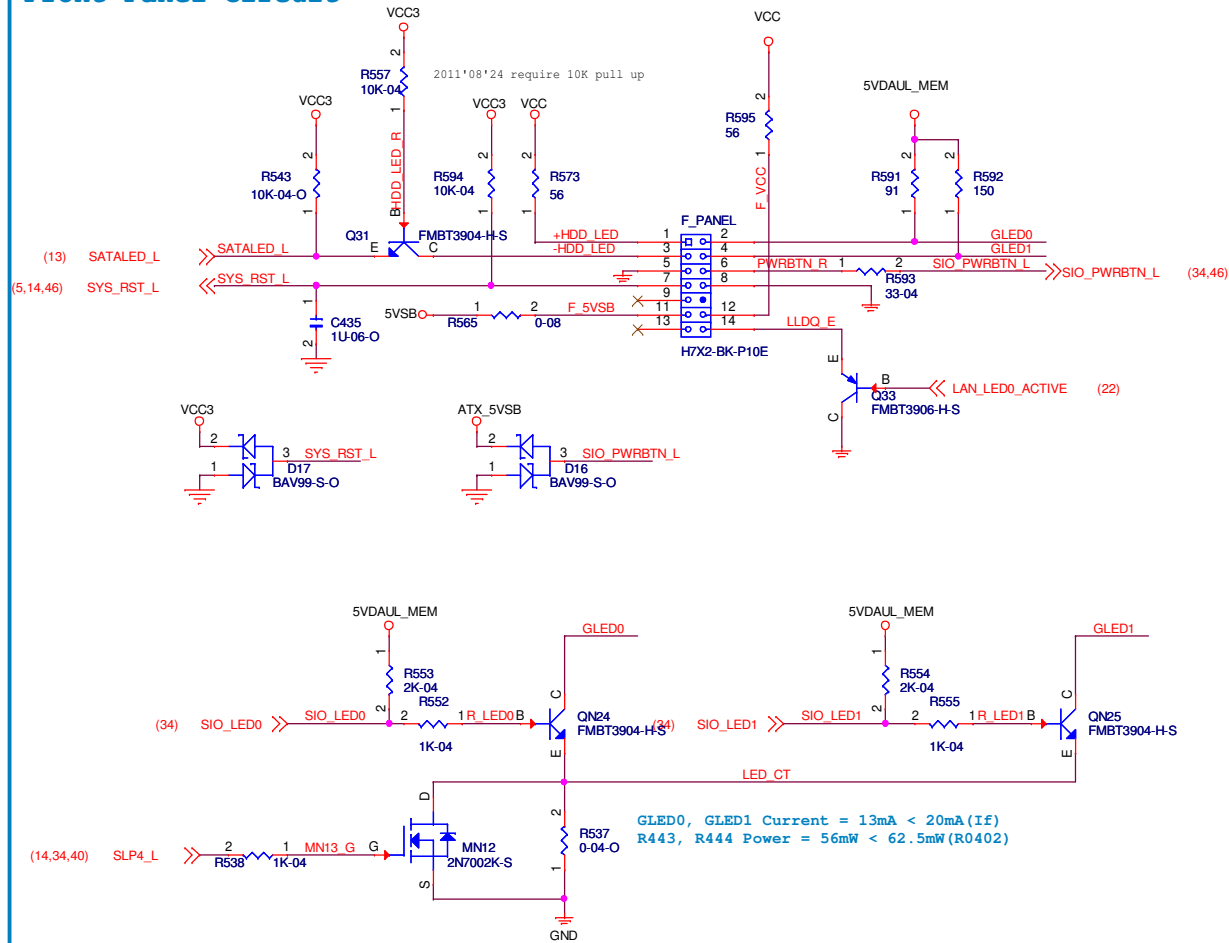
+ - terminal add short pad to ground for nonuse OP , 20110406

**ECS** Elitegroup Computer Systems

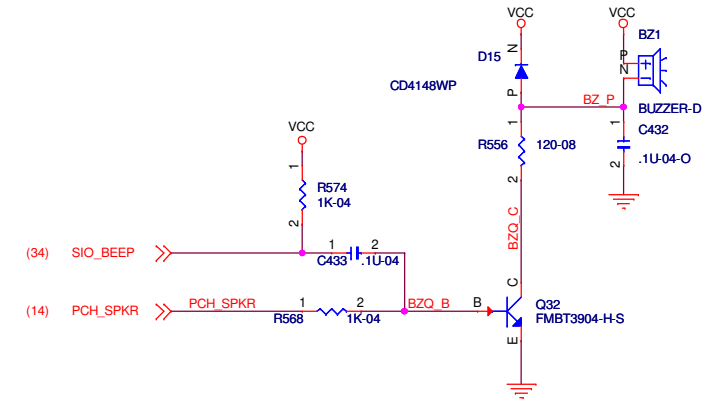
Title	FAN, COM		
Size	Document Number	Rev	
Custom	Q77H2-AD	1.0.	
Date:	Tuesday, April 10, 2012	Sheet	36 of 49



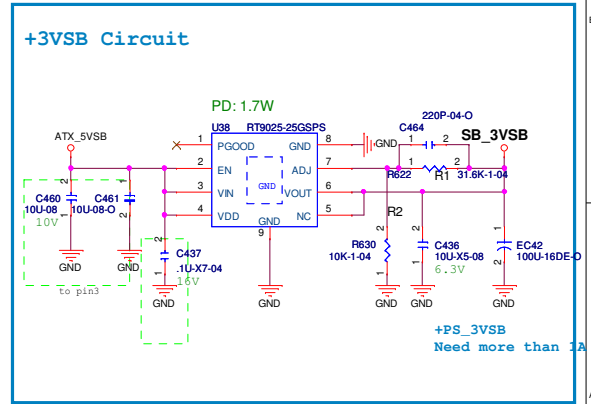
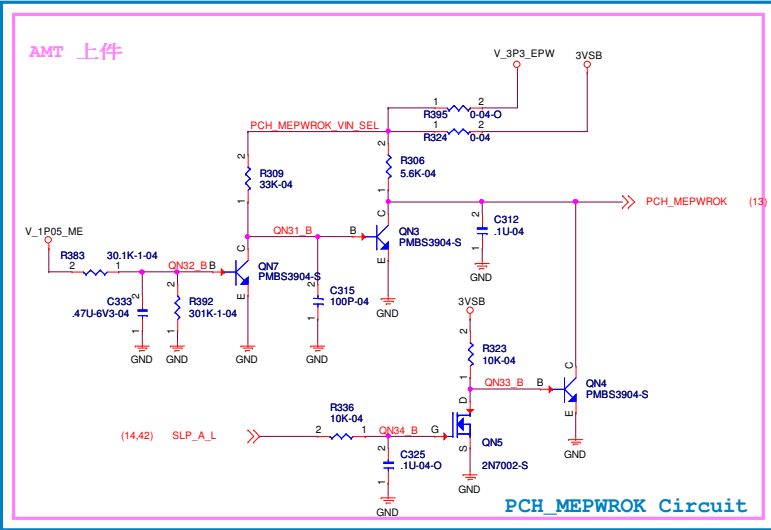
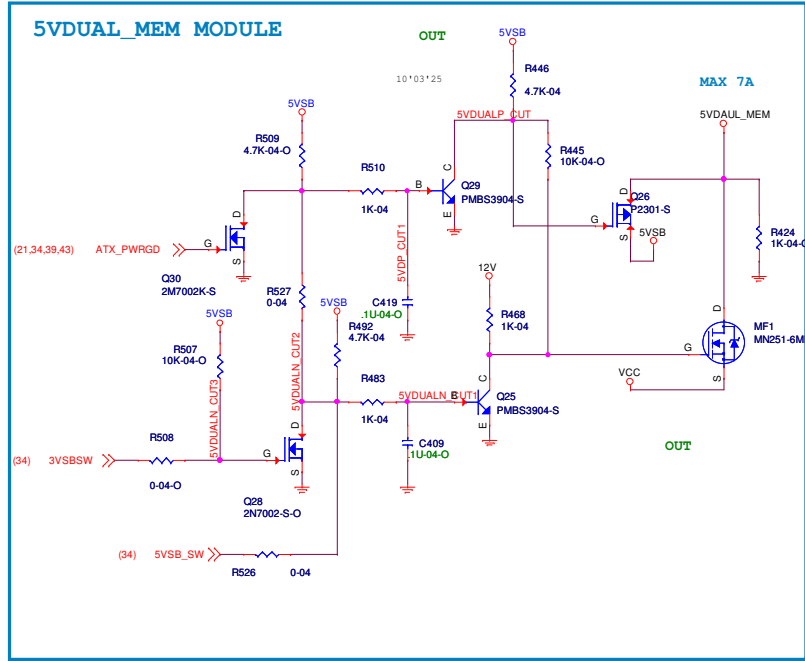
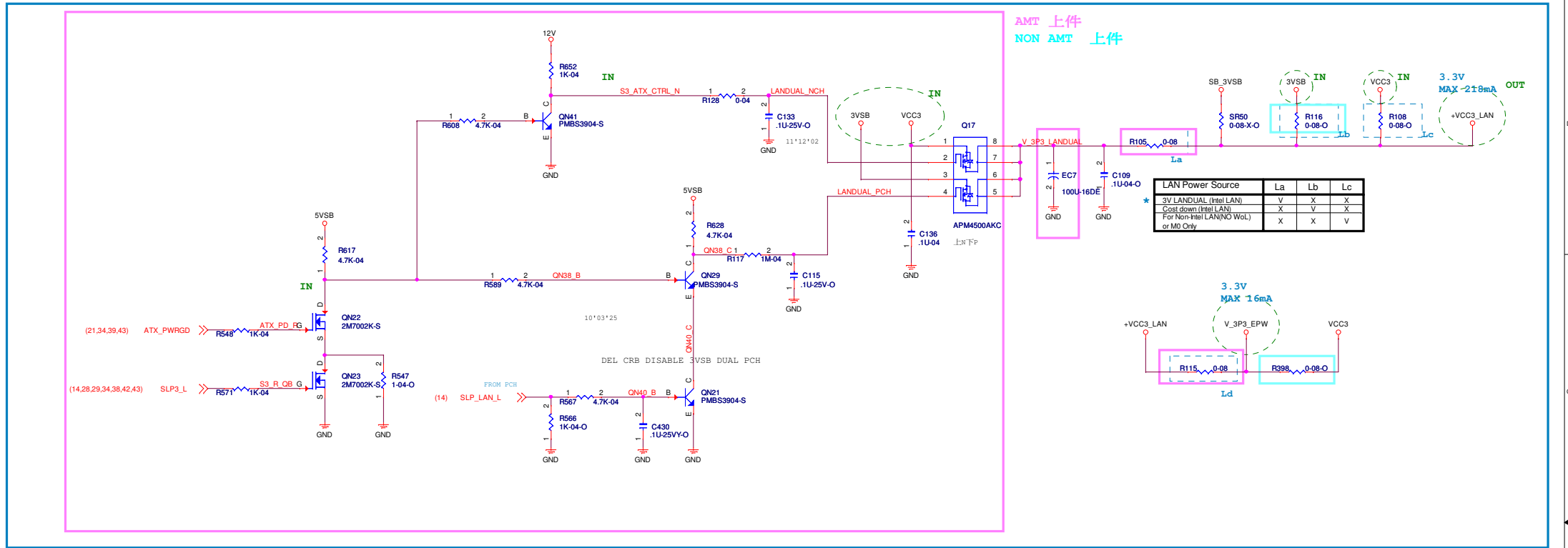
## Front Panel Circuit



## Buzzer Circuit



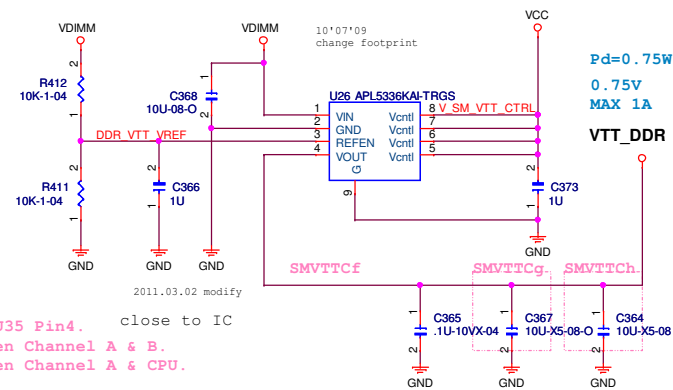




<b>SLP4_L</b>	<b>High</b>	<b>Low</b>
<b>NCP1587DR2G</b>	<b>Enable</b>	<b>Disable</b>

[illegible]

## AP5336/GS9020/AME9172M



Layout Note:  
SMVTTc close to U35 Pin4.  
SMVTTcG are between Channel A & B.  
SMVTTCh are between Channel A & CPU.

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



- $I_{SS}$  is the soft-start current source at the 20 $\mu$ A limit
- $V_{SREF}$  is the buffered  $V_{REF}$  reference voltage

Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V <sub>SREF</sub>	V <sub>OUT</sub>
1	1	SW0	V <sub>SET1</sub>	V <sub>OUT1</sub>
1	0	SW1	V <sub>SET2</sub>	V <sub>OUT2</sub>
0	1	SW2	V <sub>SET3</sub>	V <sub>OUT3</sub>
0	0	SW3	V <sub>SET4</sub>	V <sub>OUT4</sub>

The ISL95870B  $V_{SET1}$  setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (\text{EQ. 21})$$

The ISL95870B  $V_{SET3}$  setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left( 1 + \frac{R_{SET1} + R_{SET2}}{R} \right) \quad (\text{EQ. 23})$$

The ISL95870B  $V_{SET4}$  setpoint is written as Equation 24:

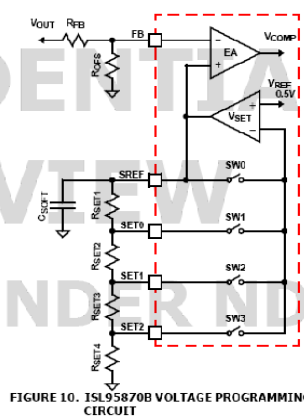
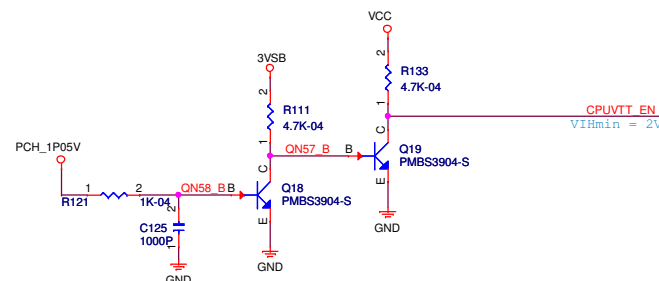
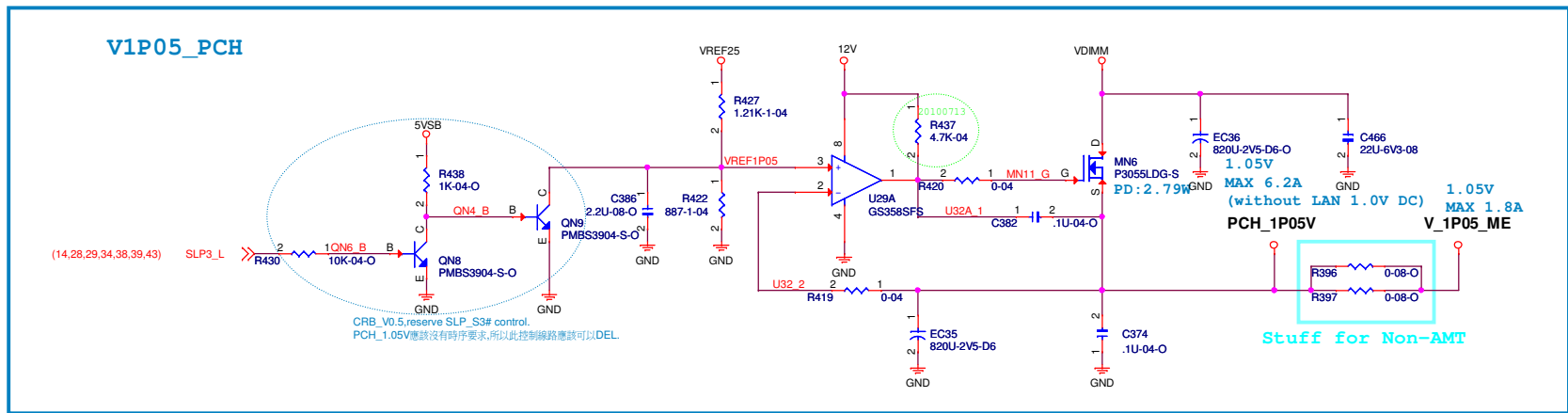
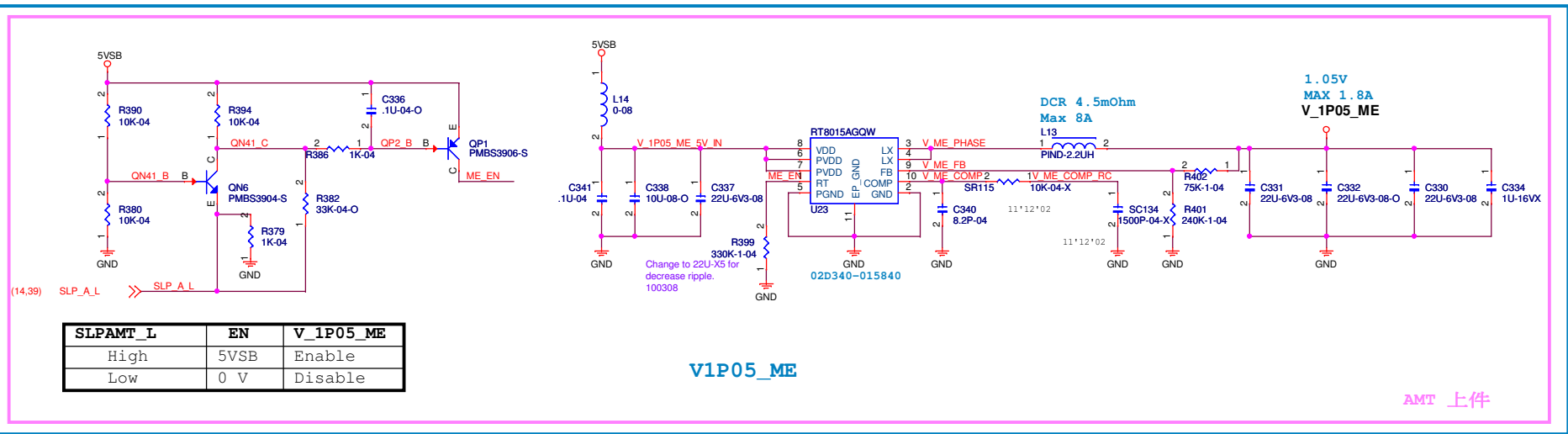


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT





**BOM Note:**

02-340-015840...dn10\_r18106a  
IC REG.RT8015AGQW.WDFN 10P.3A. LEAD-FREE(RoHS/HF).  
RICHTER

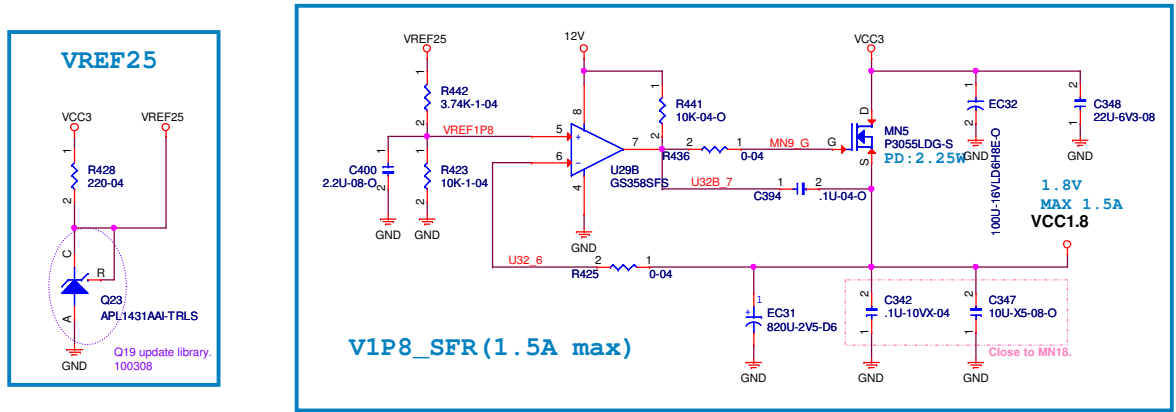
08-413-225094...choke\_2r2m\_pt4d9x4d6mm  
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2\*8.2\*7.5\*6.7  
mm.AKL0806MN-2R2M-L3.2...LEAD-FREE(RoHS).MAGIC

05-152-750113  
RES.75K.1/16W.1%.SMD 0402.....LEAD-FREE(RoHS/HF).

05-152-430103  
RES.43K.1/16W.5%.SMD 0402.....LEAD-FREE(RoHS/HF).

05-152-240114  
RES.240K.1/16W.1%.SMD 0402.....LEAD-FREE(RoHS/HF).

04-880-828100  
C/C.8.2pF.50V.0.25pl..NPO...SMD 0402....LEAD-FREE(RoHS/HF).



# Default Stuffed:

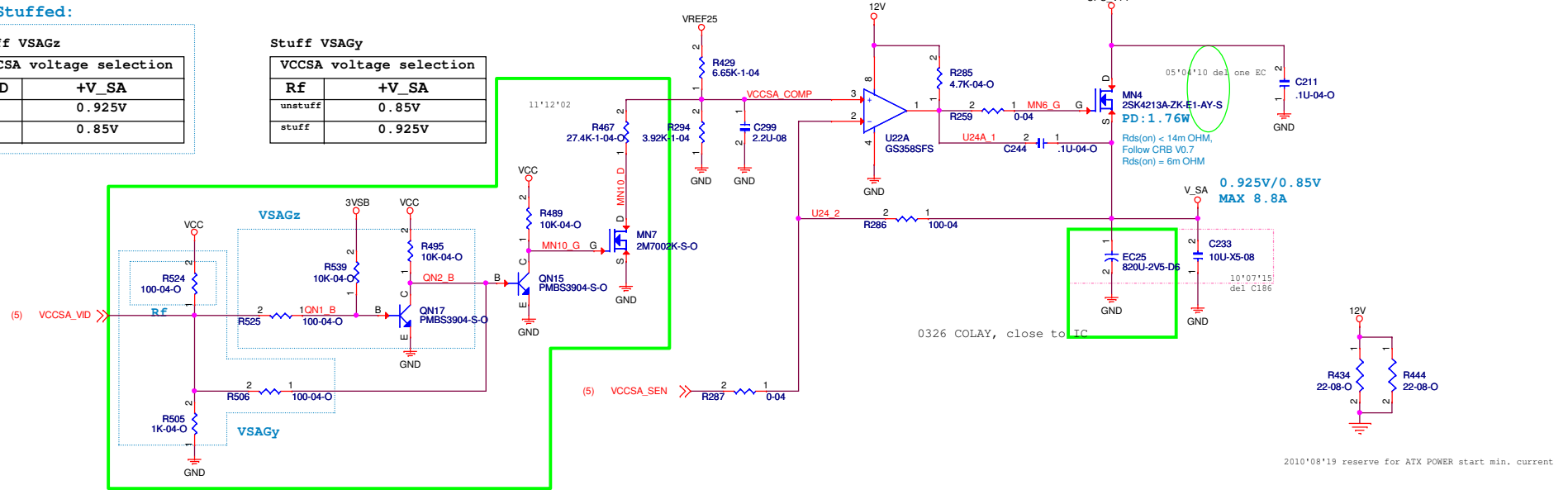
## Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

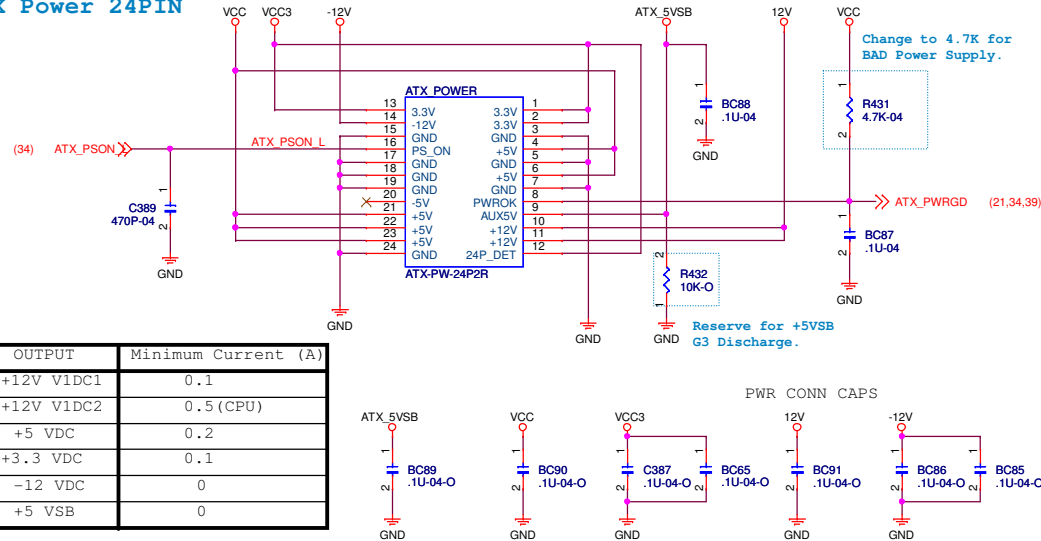
★

## Stuff VSAGy

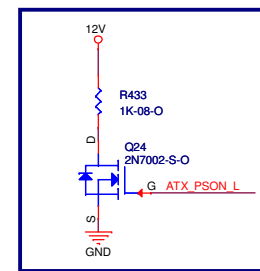
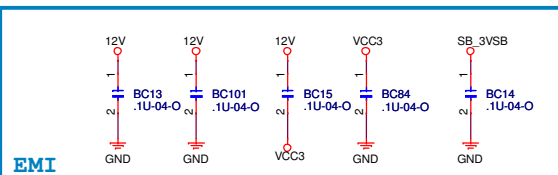
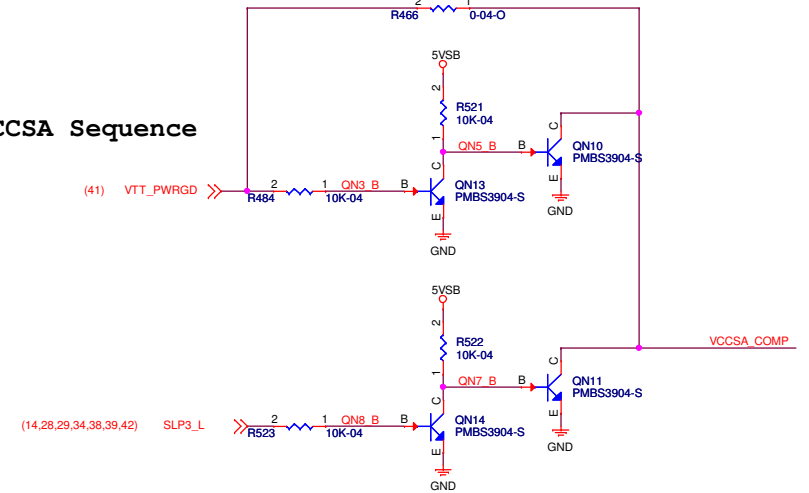
VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



## ATX Power 24PIN



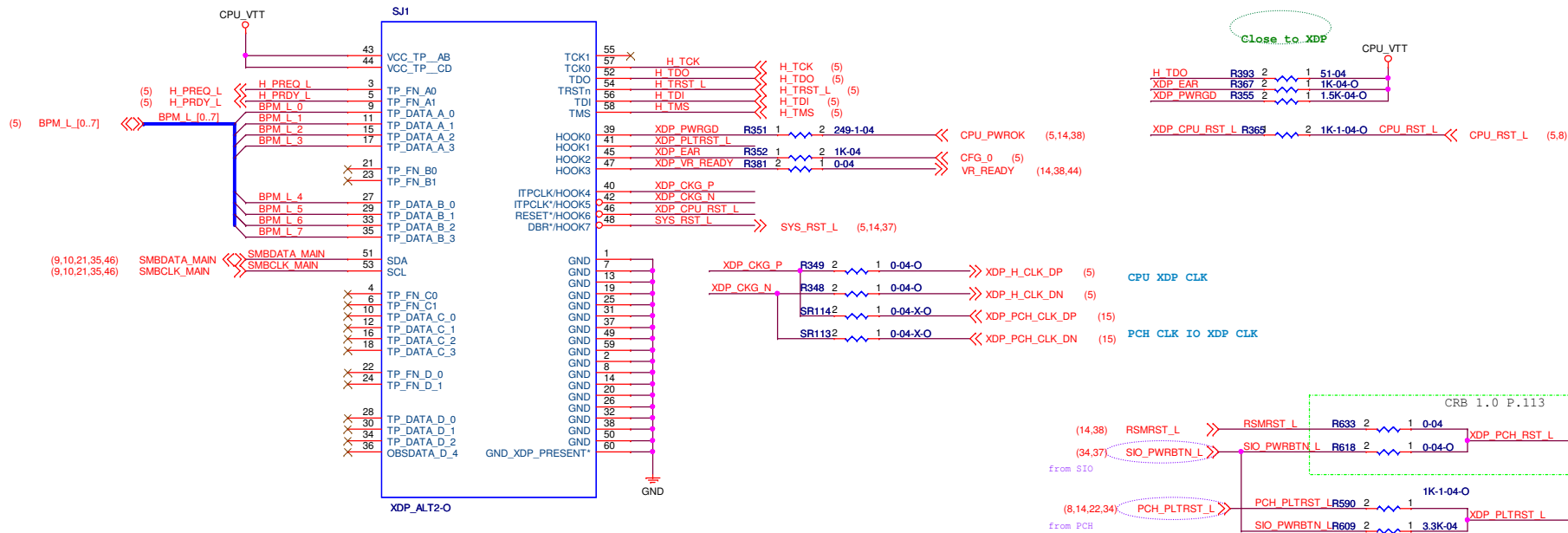
## VCCSA Sequence











DESIGN NOTE:  
PCH JTAG

DESIGN NOTE:  
DEFENSIVE DESIGN



